
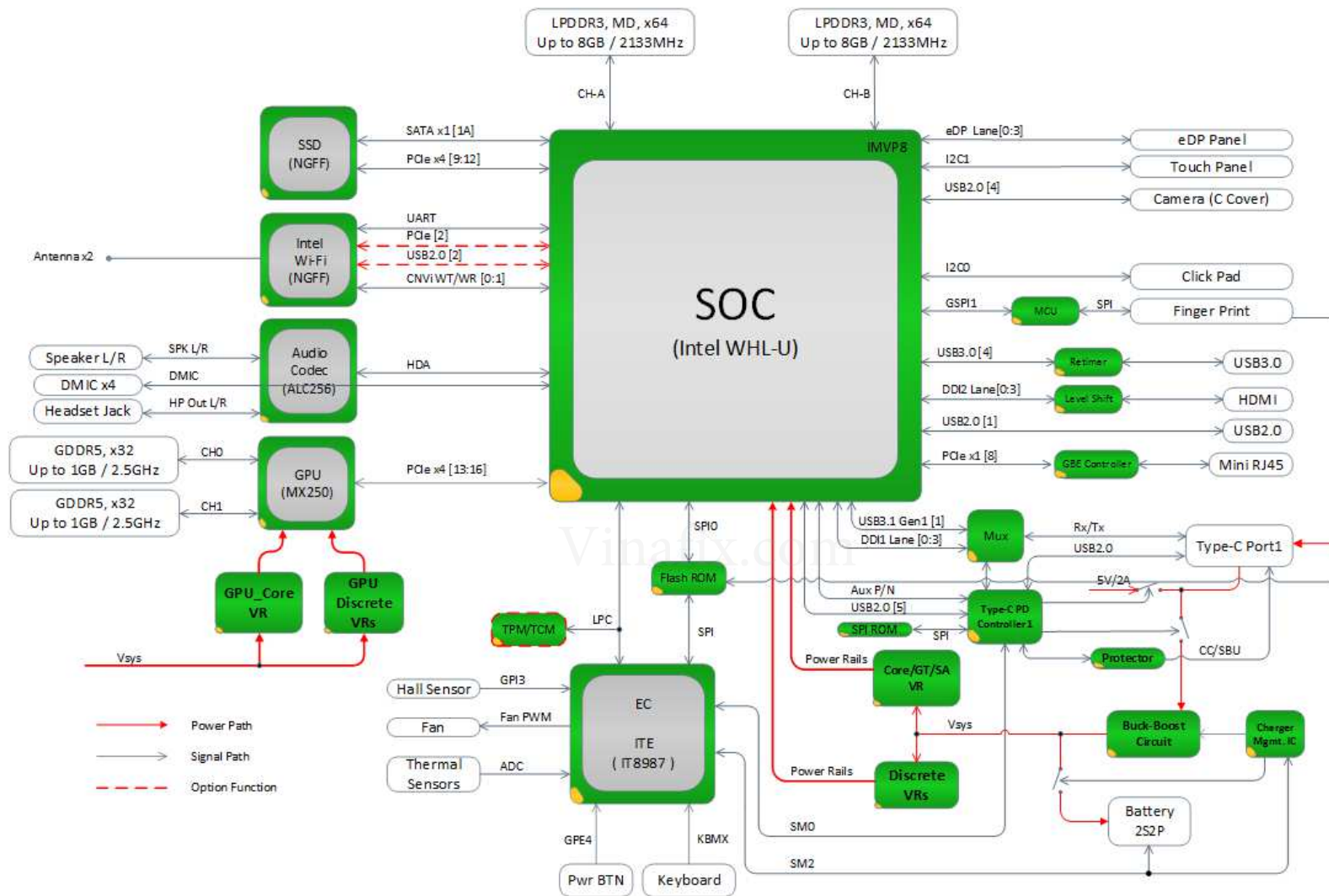
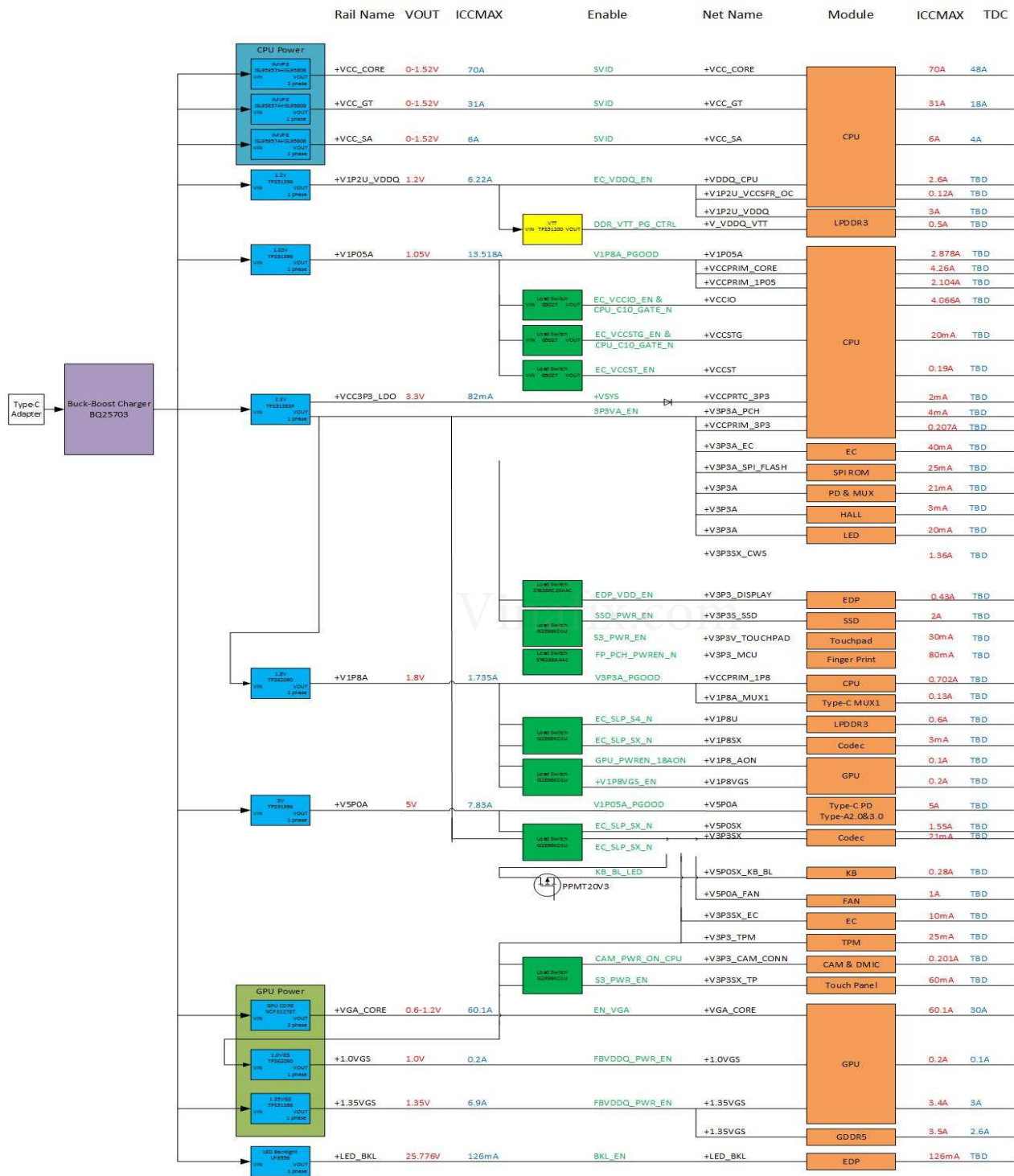


Schematics Page Index (Title / Revision / Change Date)

Page	Title of Schematics Page	Rev.	Date	Page	Title of Schematics Page	Rev.	Date
01	Index	1.0		35	EDP & CAM & TP	1.0	
02	Block Diagram	1.0		36	HDMI	1.0	
03	Power Map	1.0		37	Codec	1.0	
04	I2C Table	1.0		38	M.2 SSD	1.0	
05	Blank	1.0		39	WLAN WIFI BT MODULE	1.0	
06	WHL-U42 (CHA)	1.0		40	Speaker CONN	1.0	
07	WHL-U42 (CHB)	1.0		41	KB CON & Backlight	1.0	
08	WHL-U42 (DISPLAY)	1.0		42	EC (IT8987E)	1.0	
09	WHL-U42 (SPI/LPC/ESPI/XDP)	1.0		43	BUTTON/FAN/LED/Hall	1.0	
10	WHL-U42 (CNV1/EMMC/CLK)	1.0		44	TouchPad	1.0	
11	WHL-U42 (HDA/SD/I2C/GPIO)	1.0		45	MCP&Finger Print conn	1.0	
12	WHL-U42 (USB/PCIE)	1.0		46	RSMRST OFF	1.0	
13	WHL-U42 (PMU)	1.0		47	N17S PCIE/ CLK/ GPIO	1.0	
14	WHL-U42 (VCORE/GT)	1.0		48	N17S DISPLAY/ STRAP/ JTAG	1.0	
15	WHL-U42 (PCH)	1.0		49	N17S MEM Power	1.0	
16	WHL-U42 (VCC/VDDQ)	1.0		50	N17S +VGA CORE, GND	1.0	
17	WHL-U42 (VSS)	1.0		51	N17S MEM Interface	1.0	
18	WHL-U42 (CFG)	1.0		52	N17S GDDR5	1.0	
19	WHL-U42 (DECOUPLING1)	1.0		53	N17S MISC	1.0	
20	WHL-U42 (DECOUPLING2)	1.0		54	sensor	1.0	
21	WHL-U42 (DECOUPLING3)	1.0		55	TPM	1.0	
22	WHL-U42 (DECOUPLING4)	1.0		56	POWER DCIN & BATTERY CHARGER	1.0	
23	LPDDR3 CH-A 1	1.0		57	POWER DELIVERY 3.3V	1.0	
24	LPDDR3 CH-A 2	1.0		58	POWER DELIVERY 5V	1.0	
25	LPDDR3 CH-B 1	1.0		59	POWER DELIVERY 1.8V	1.0	
26	LPDDR3 CH-B 2	1.0		60	POWER DELIVERY 1.05V	1.0	
27	LPDDR3 (DECAPS)	1.0		61	POWER DELIVERY-IMVP1	1.0	
28	LPDDR3 TERMINATIONS	1.0		62	POWER DELIVERY 1.2V	1.0	
29	SYSTEM FLASH	1.0		63	POWER DELIVERY 1.35VGS	1.0	
30	TYPE1-C CONN	1.0		64	POWER DELIVERY 1.0VGS&1.8VGS	1.0	
31	TYPE1-C PD & MUX	1.0		65	POWER DELIVERY-GPU Core	1.0	
32	USB3.0&2.0	1.0		66	POWER DELIVERY Load switch	1.0	
33	LAN	1.0		67	LED BACKLIGHT	1.0	
34	BLANK	1.0		68	Debug Conn	1.0	
				69	Hole & Mark	1.0	
				70	Changelist	1.0	

 HUAQIN 华勤通信		FOXCONN
Page name: Index		
Size: A4	Project Name: MATEBOOK 14	REV: V1.0
Date: Saturday, December 15, 2018	Sheet: 1	of 74




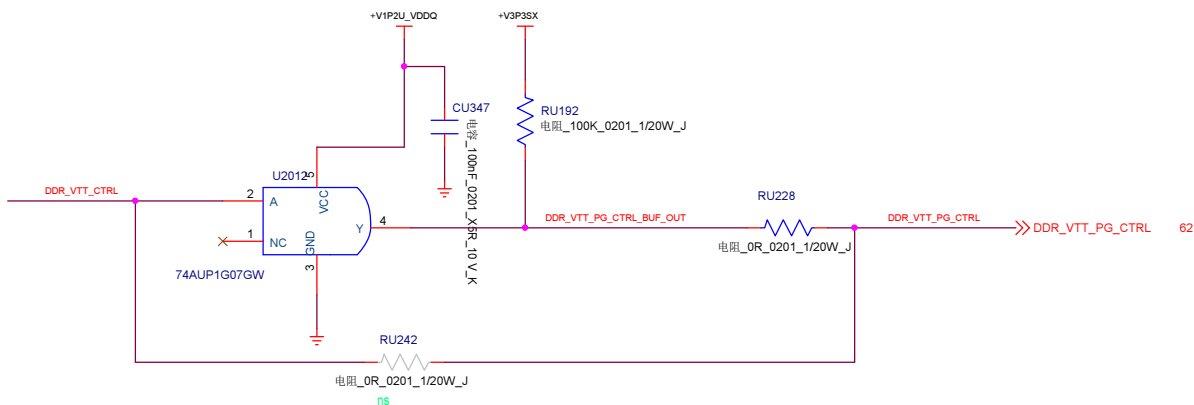


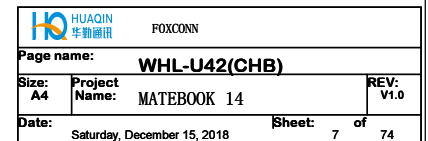
I2C Allocation Mapping

EC	Device1		Device2			Device3
SMCLK0	Type-C1(PD)	0x40	x	x	x	x
SMDAT0						
SMCLK1	Battery	0x16	x	x	x	x
SMDAT1						
SMCLK2	Charger	0xD6	GPU	0x9E	LCD Back Light	0x58
SMDAT2						
SMCLK3	Debug	address:TBD	x	x	x	x
SMDAT3						
SOC	Device1		Device2		Device3	
I2C_CLK0	TOUCHPAD	0x15	X	X	X	X
I2C_DAT0						
I2C_CLK1	TOUCHPAENL	0x10	X	X	X	X
I2C_DAT1						
I2C_CLK2	X	X	X	X	X	X
I2C_DAT2						
I2C_CLK3	X	X	X	X	X	X
I2C_DAT3						
I2C_CLK4	X	X	X	X	X	X
I2C_DAT4						
I2C_CLK4B	X	X	X	X	X	X
I2C_DAT4B						
ISH_I2C_CLK0	X	X	X	X	X	X
ISH_I2C_DAT0						
ISH_I2C_CLK1	X	X	X	X	X	X
ISH_I2C_DAT1						
ISH_I2C_CLK2	X	X	X	X	X	X
ISH_I2C_DAT2						

Vinafix.com

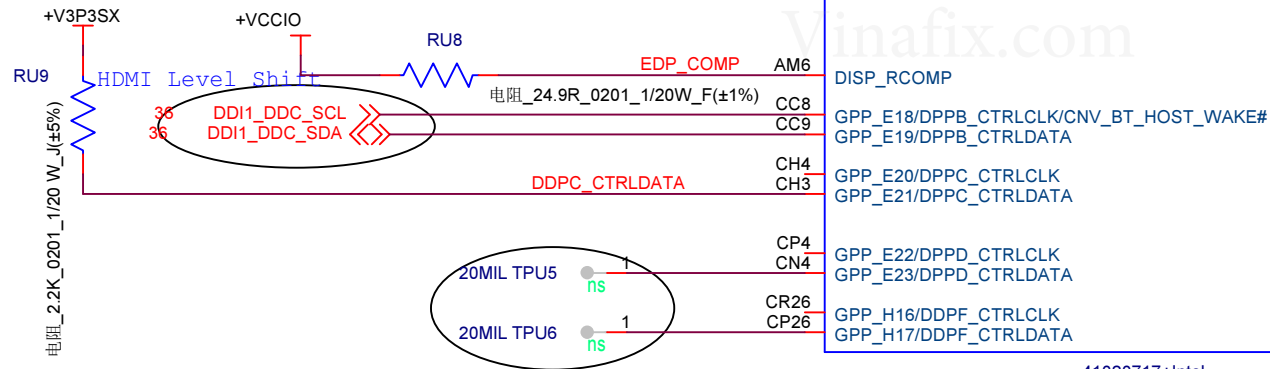
		FOXCONN	
Page name: Blank			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 5	of 74	





HDMI DDI

TypeC DP DDI



UU1A

AL5
AL6
AJ5
AJ6
AF6
AF5
AE5
AE6

AC4
AC3
AC1
AC2
AE4
AE3
AE1
AE2

DDI1_TXN_0
DDI1_TXP_0
DDI1_TXN_1
DDI1_TXP_1
DDI1_TXN_2
DDI1_TXP_2
DDI1_TXN_3
DDI1_TXP_3

EDP_TXN_0
EDP_TXP_0
EDP_TXN_1
EDP_TXP_1
EDP_TXN_2
EDP_TXP_2
EDP_TXN_3
EDP_TXP_3

EDP_AUX
EDP_AUX_P

DISP_UTILS

DDI1_AUX
DDI1_AUX_P
DDI2_AUX
DDI2_AUX_P
DDI3_AUX
DDI3_AUX_P

GPP_E13/DDPB_HPD0/DISP_MISC0
GPP_E14/DDPC_HPD1/DISP_MISC1
GPP_E15/DPPD_HPD2/DISP_MISC2
GPP_E16/DPPE_HPD3/DISP_MISC3
GPP_E17/EDP_HPD/DISP_MISC4

EDP_BKLTEN
EDP_VDDEN
EDP_BKLTCTL

DISP_RCOMP

GPP_E18/DPPB_CTRLCLK/CNV_BT_HOST_WAKE#
GPP_E19/DPPB_CTRLDATA

GPP_E20/DPPC_CTRLCLK
GPP_E21/DPPC_CTRLDATA

GPP_E22/DPPD_CTRLCLK
GPP_E23/DPPD_CTRLDATA

GPP_H16/DDPF_CTRLCLK
GPP_H17/DDPF_CTRLDATA

AG4 EDP_TX0_SOC_DN EDP_TX0_SOC_DN 35
AG3 EDP_TX0_SOC_DP EDP_TX0_SOC_DP 35
AG2 EDP_TX1_SOC_DN EDP_TX1_SOC_DN 35
AG1 EDP_TX1_SOC_DP EDP_TX1_SOC_DP 35
AJ4 EDP_TX2_SOC_DN EDP_TX2_SOC_DN 35
AJ3 EDP_TX2_SOC_DP EDP_TX2_SOC_DP 35
AJ2 EDP_TX3_SOC_DN EDP_TX3_SOC_DN 35
AJ1 EDP_TX3_SOC_DP EDP_TX3_SOC_DP 35

AH4 EDP_AUX_SOC_DN EDP_AUX_SOC_DN 35
AH3 EDP_AUX_SOC_DP EDP_AUX_SOC_DP 35

AM7

AC7

AC6

AD4

AD3

AG7

AG6


CN6 DDI1_HPD DDI1_HPD 36 HPD for HDMI
CM6 DDI2_HPD DDI2_HPD 31 HPD for TypeC
CP7 SOC_SCI_N SOC_SCI_N 42 PD IC
CM7 EDP_HPD EDP_HPD 35

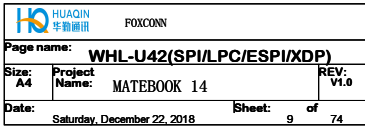
CK11 EDP_BKLT_EN EDP_BKLT_EN 35,42
CG11 EDP_VDD_EN EDP_VDD_EN 35
CH11 EDP_BKLT_PWM EDP_BKLT_PWM 35,67

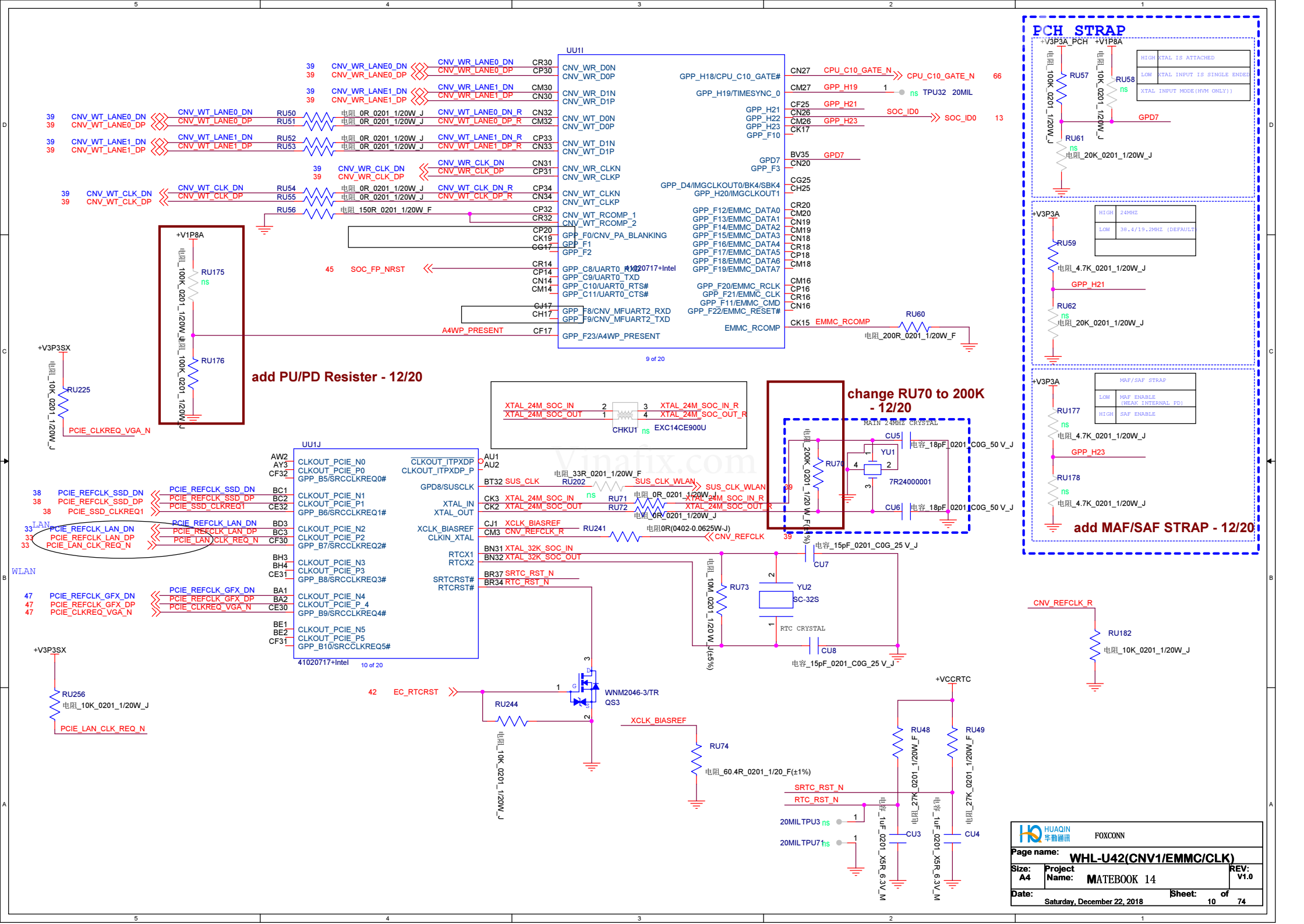
DISPLAY PORT STRAP

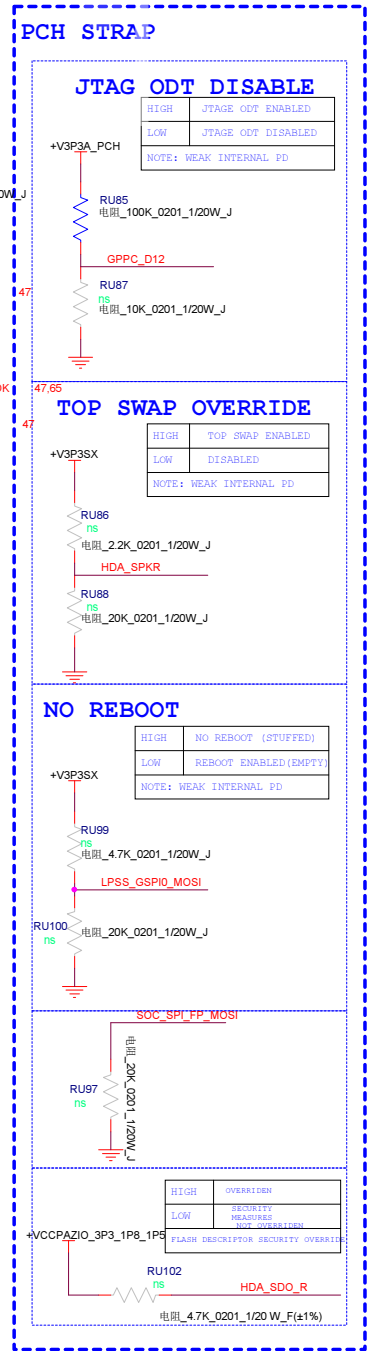
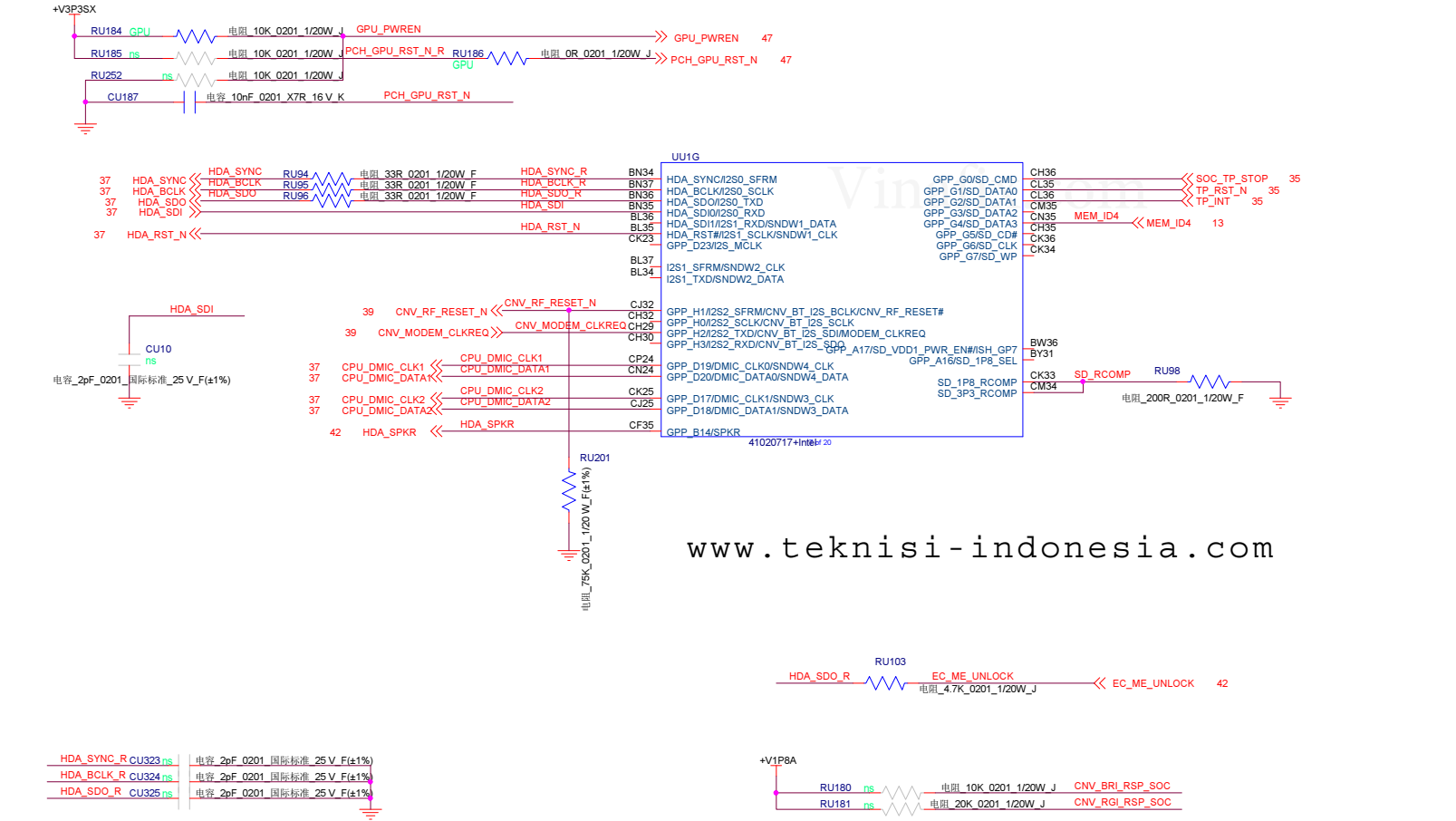
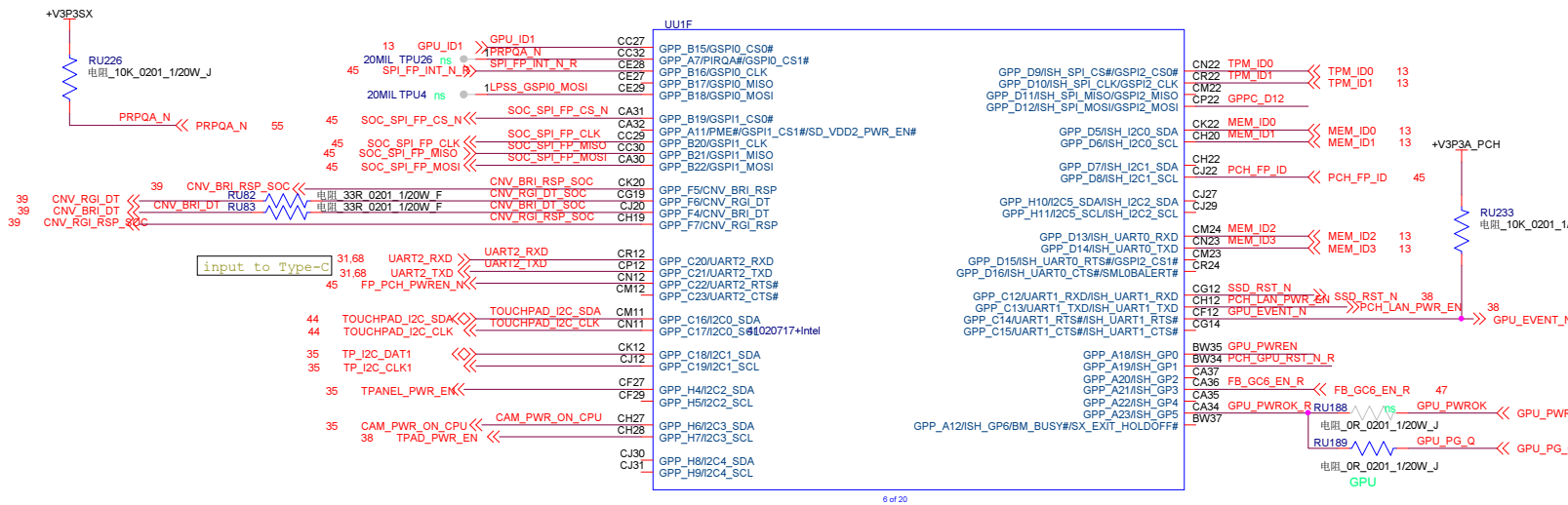
Strap	How to Enable Port	How to Disable Port	Matched HPD	DISP_RCOMP
DDI Port 1 DDPB_CTRLDATA	Pull up to 3.3 V With 2.2K	No Connect (default)	DDPB_HPD0	DISPLAY (HDMI/eDP*/DisplayPort*) 24.9Ω ±1% to VCCIO
DDI Port 2 DDPC_CTRLDATA	Pull up to 3.3 V With 2.2K (default)	No Connect	DDPC_HPD1	
eDP Port NA	NA	NA	EDP_HPD	

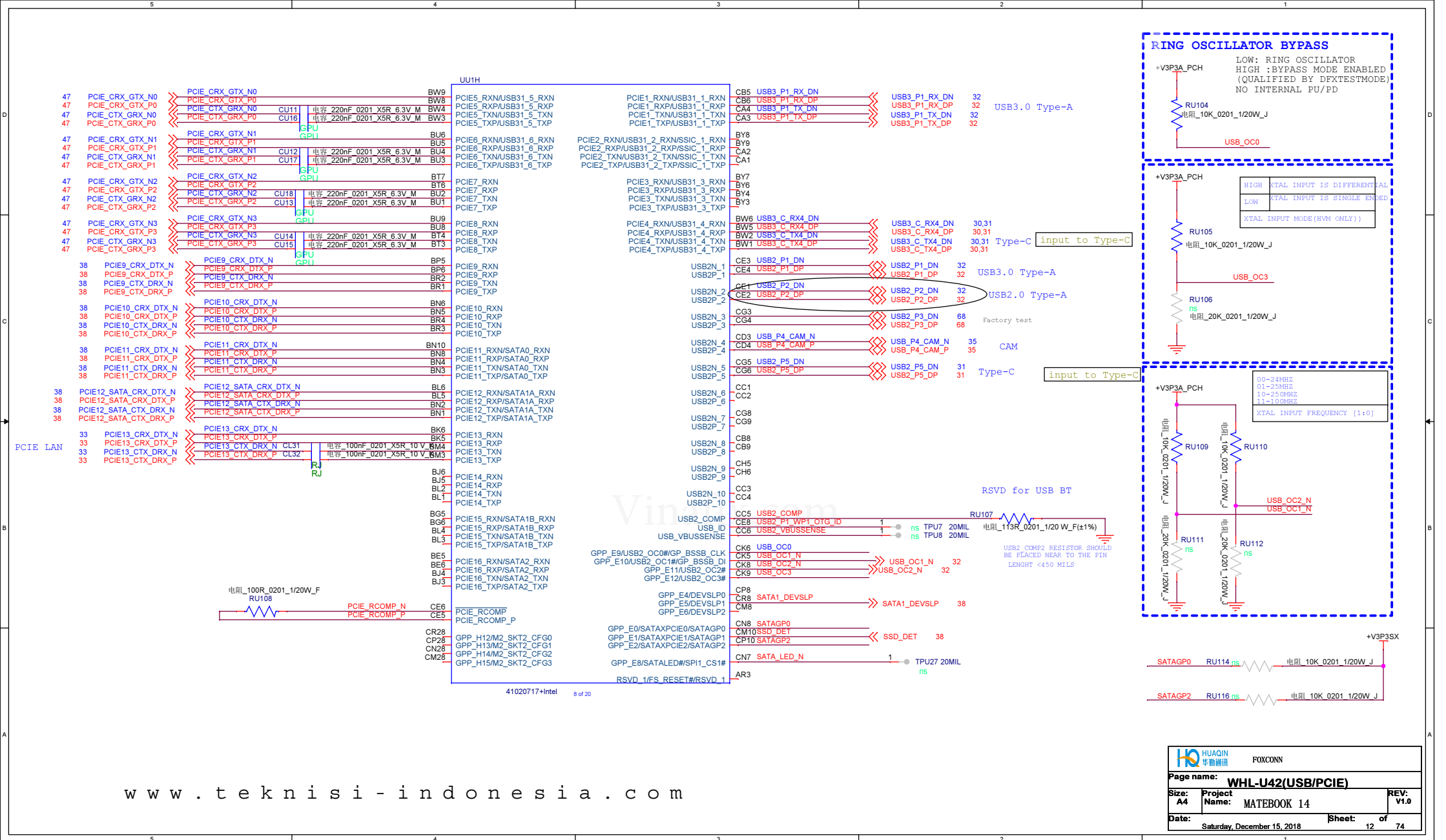
www.teknisi-indonesia.com

 HUAQIN 华勤通讯		FOXCONN	
Page name: WHL-U42(DISPLAY)			
Size: A4	Project Name: MATEBOOK 14		REV: V1.0
Date: Saturday, December 15, 2018	Sheet: 8		of 74

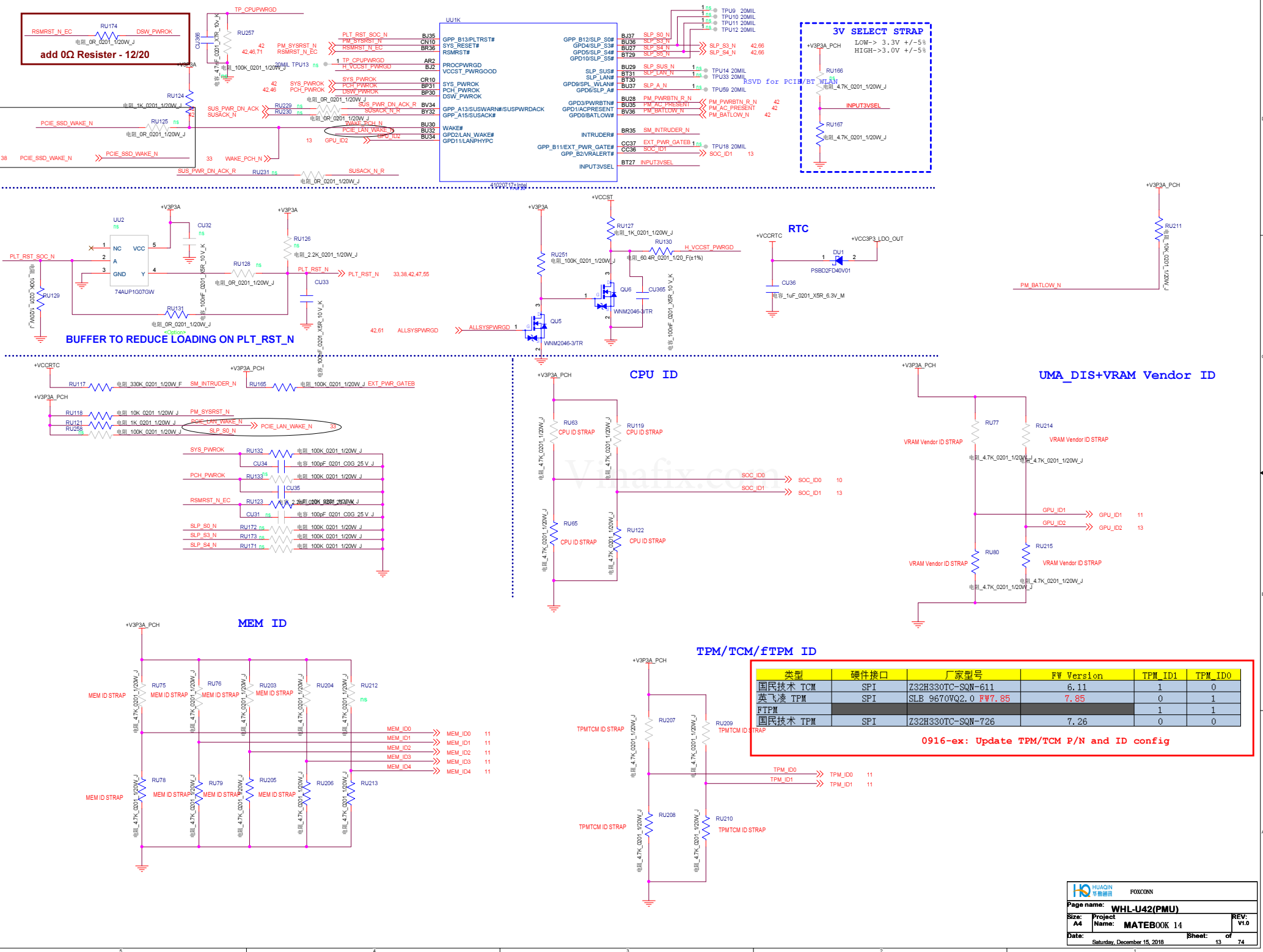






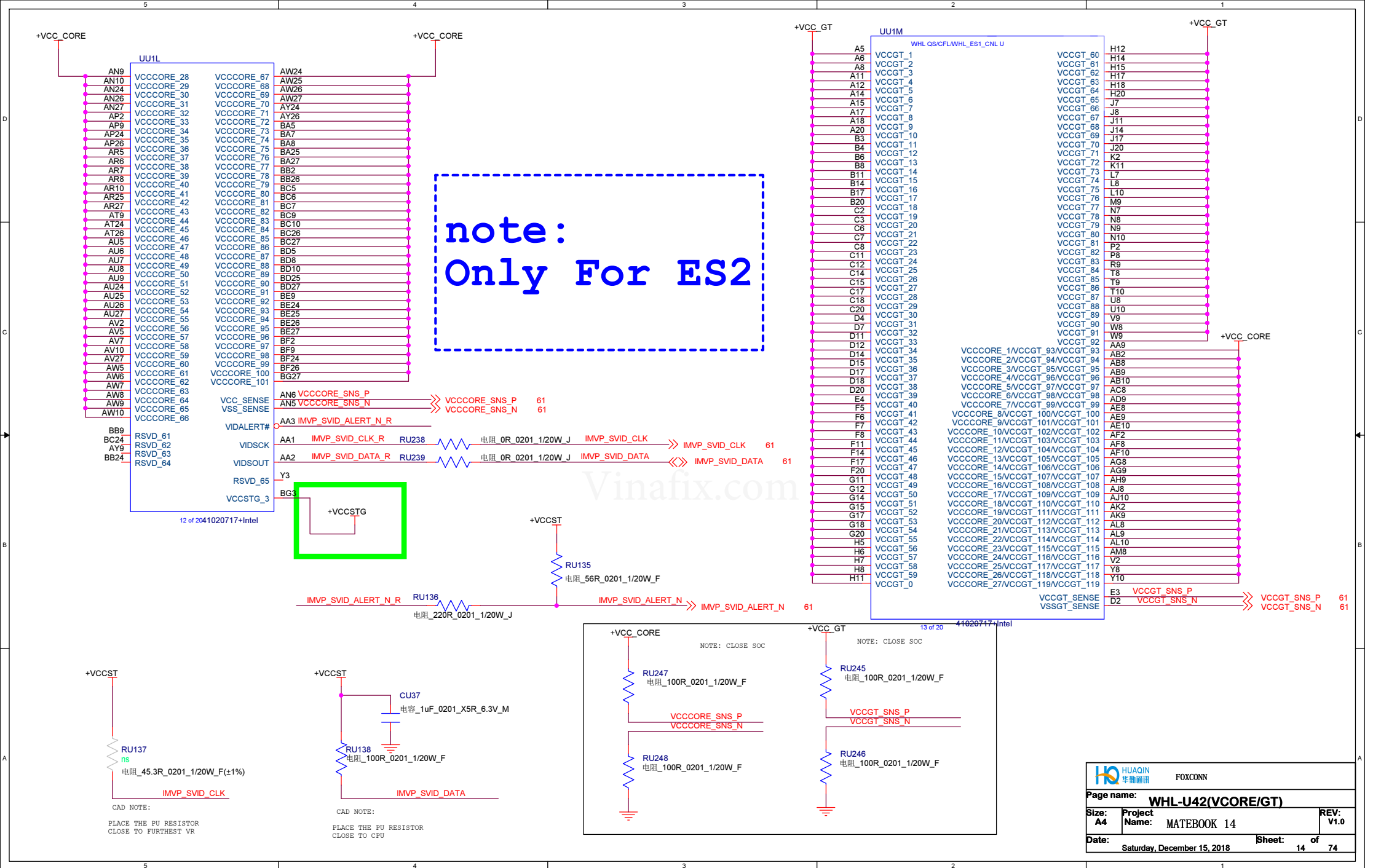


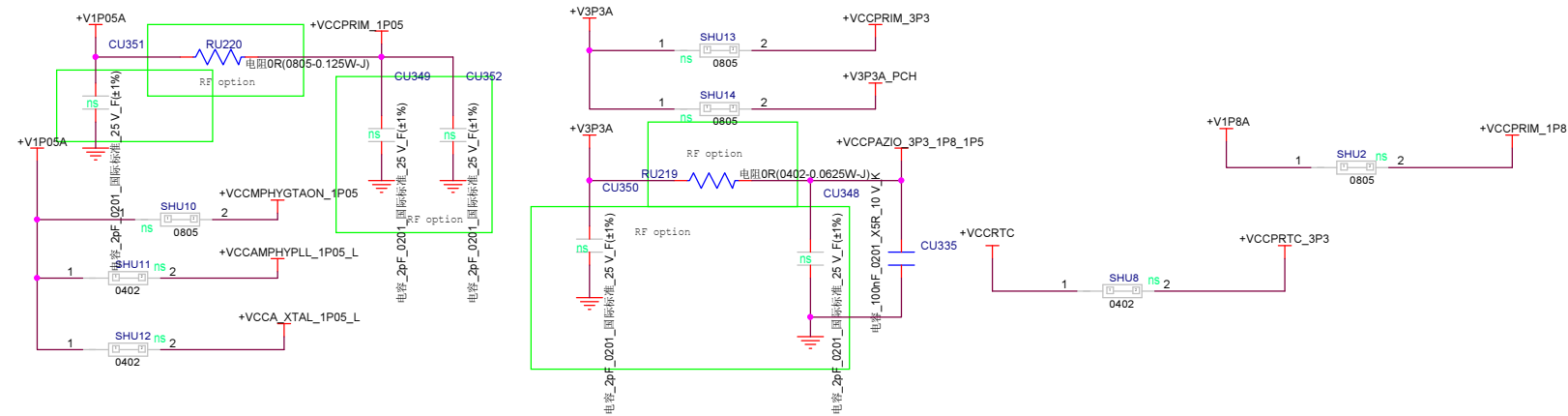
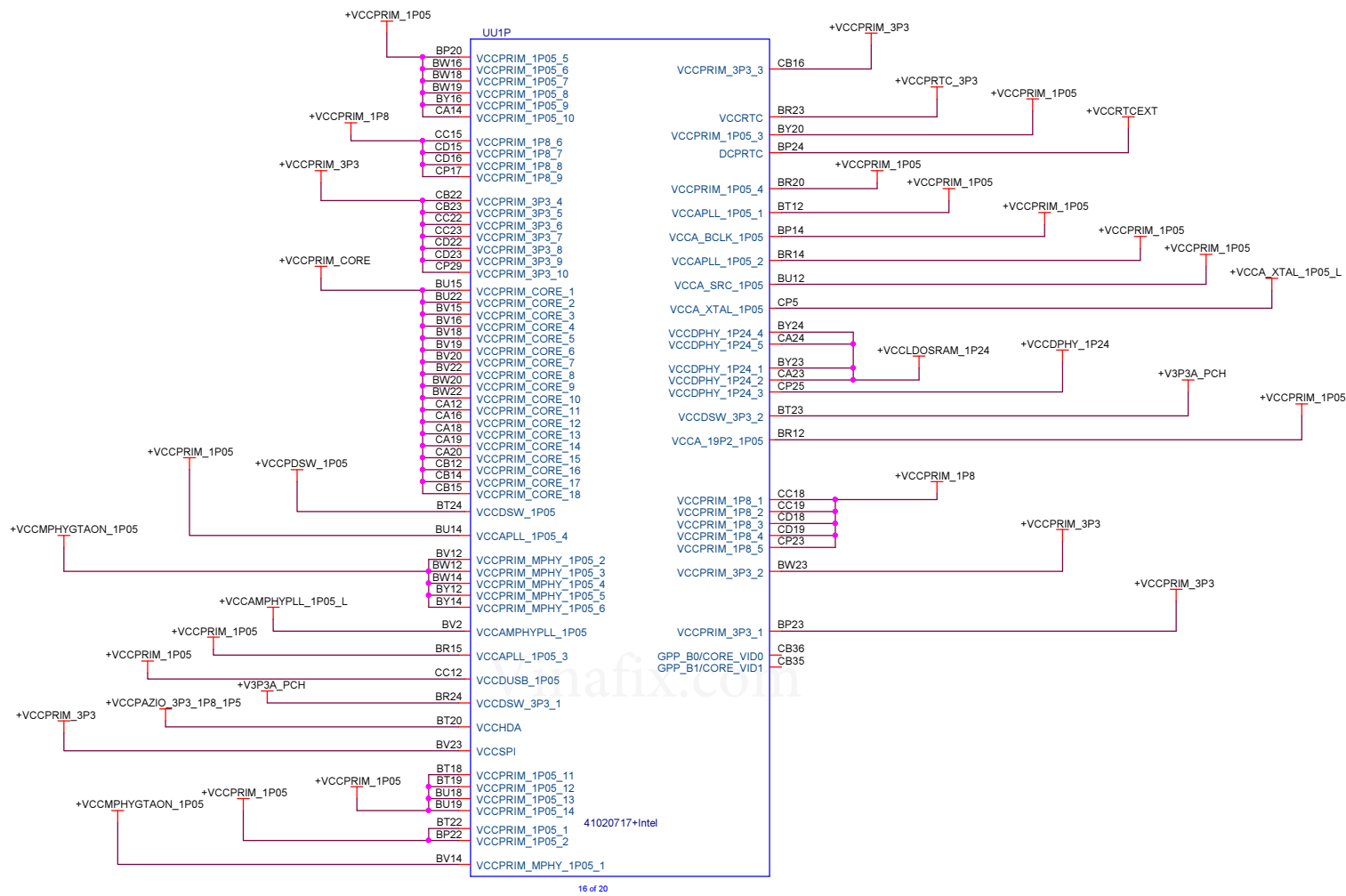
add 0Ω Resistor - 12/20

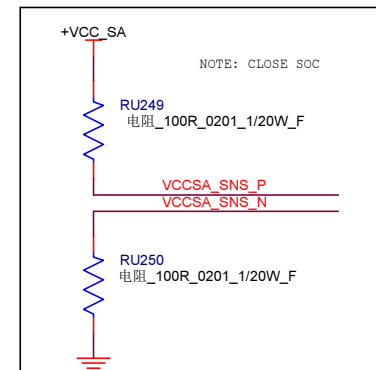
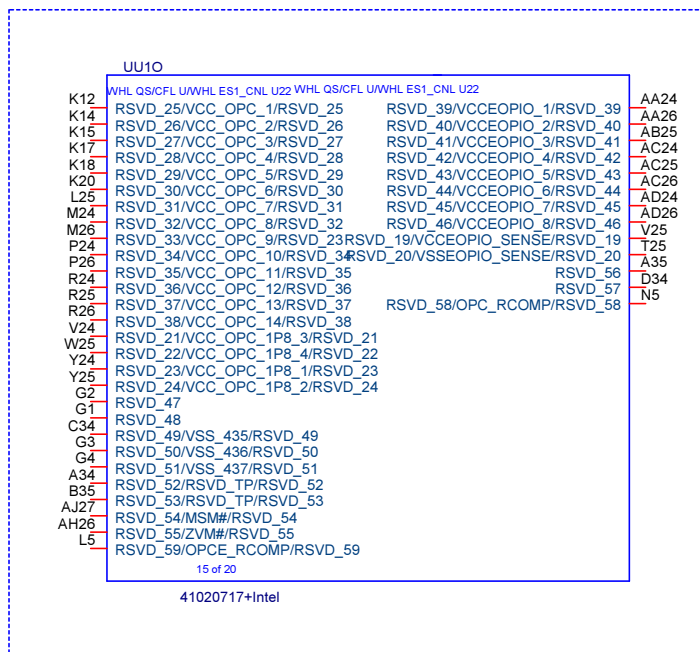
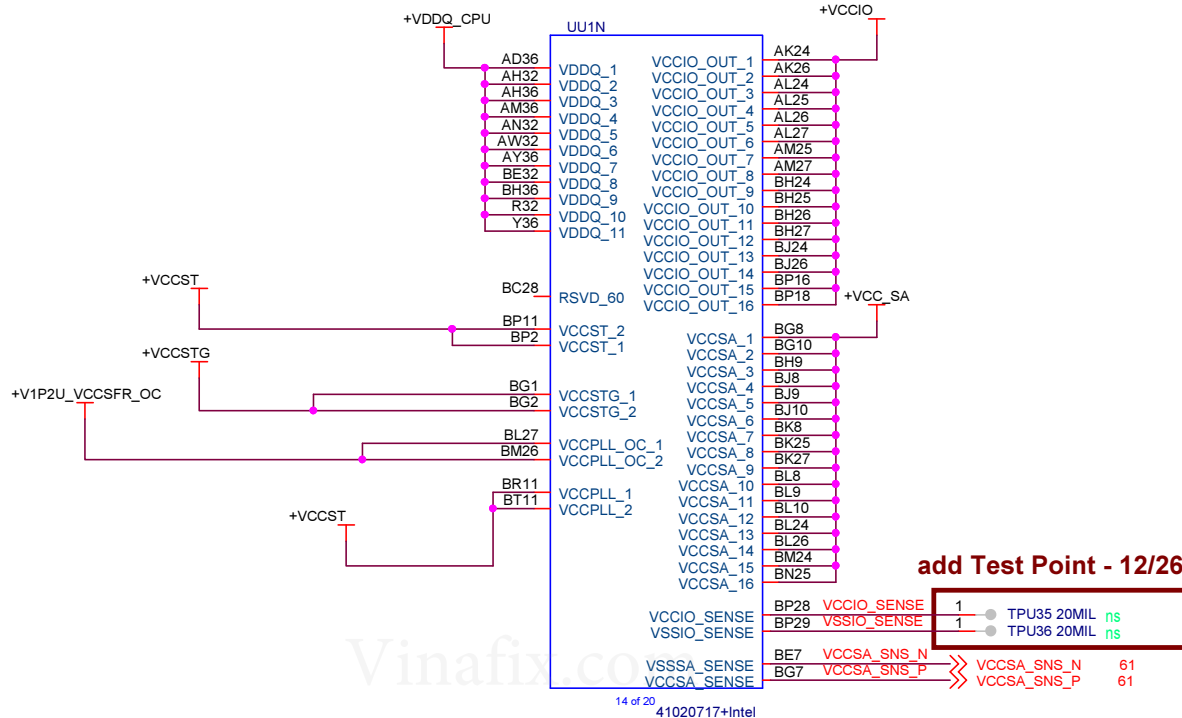
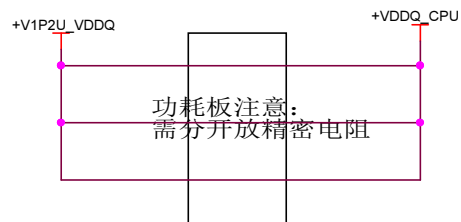


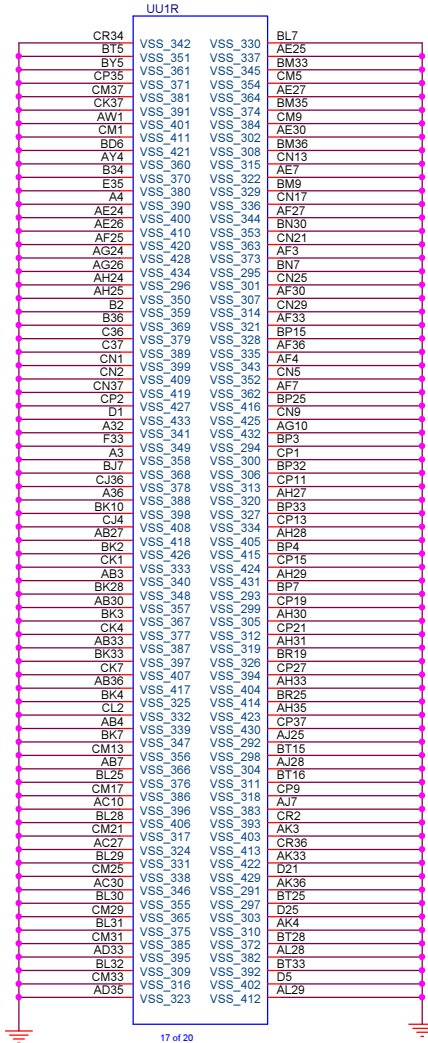
类型	硬件接口	厂家型号	FW Version	TPM_ID1	TPM_ID0
国民技术 TCM	SPI	Z32H330TC-SQN-611	6.11	1	0
英飞凌 TPM	SPI	SLB 9670VQ2.0 FW7.85	7.85	0	1
fTPM				1	1
国民技术 TPM	SPI	Z32H330TC-SQN-726	7.26	0	0

0916-ex: Update TPM/TCM P/N and ID config

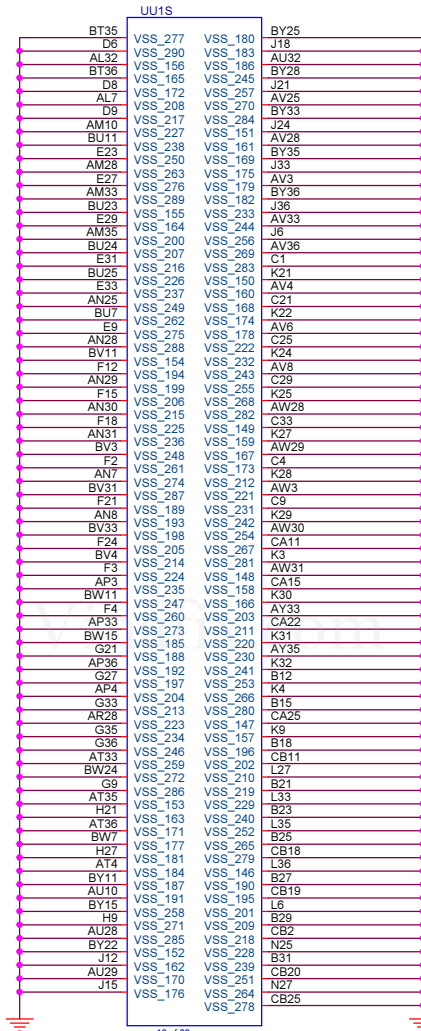




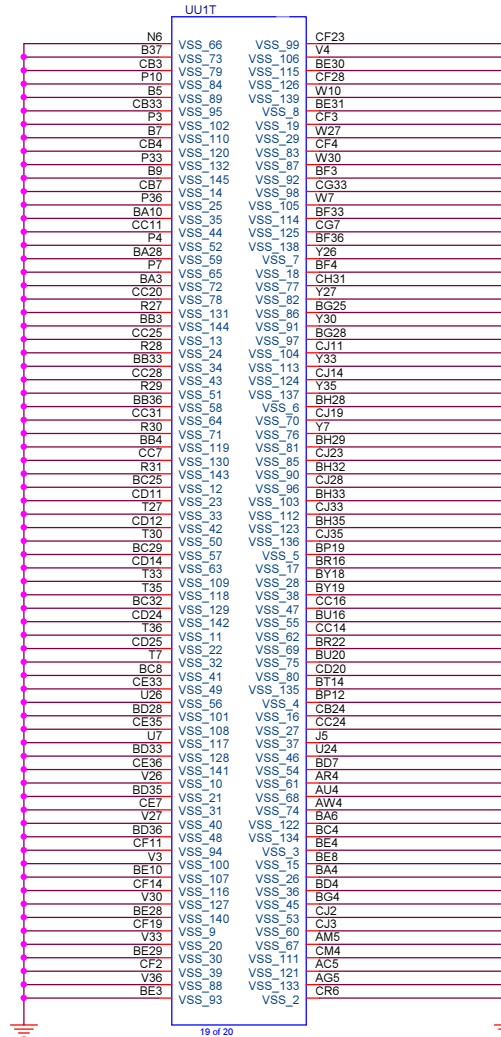




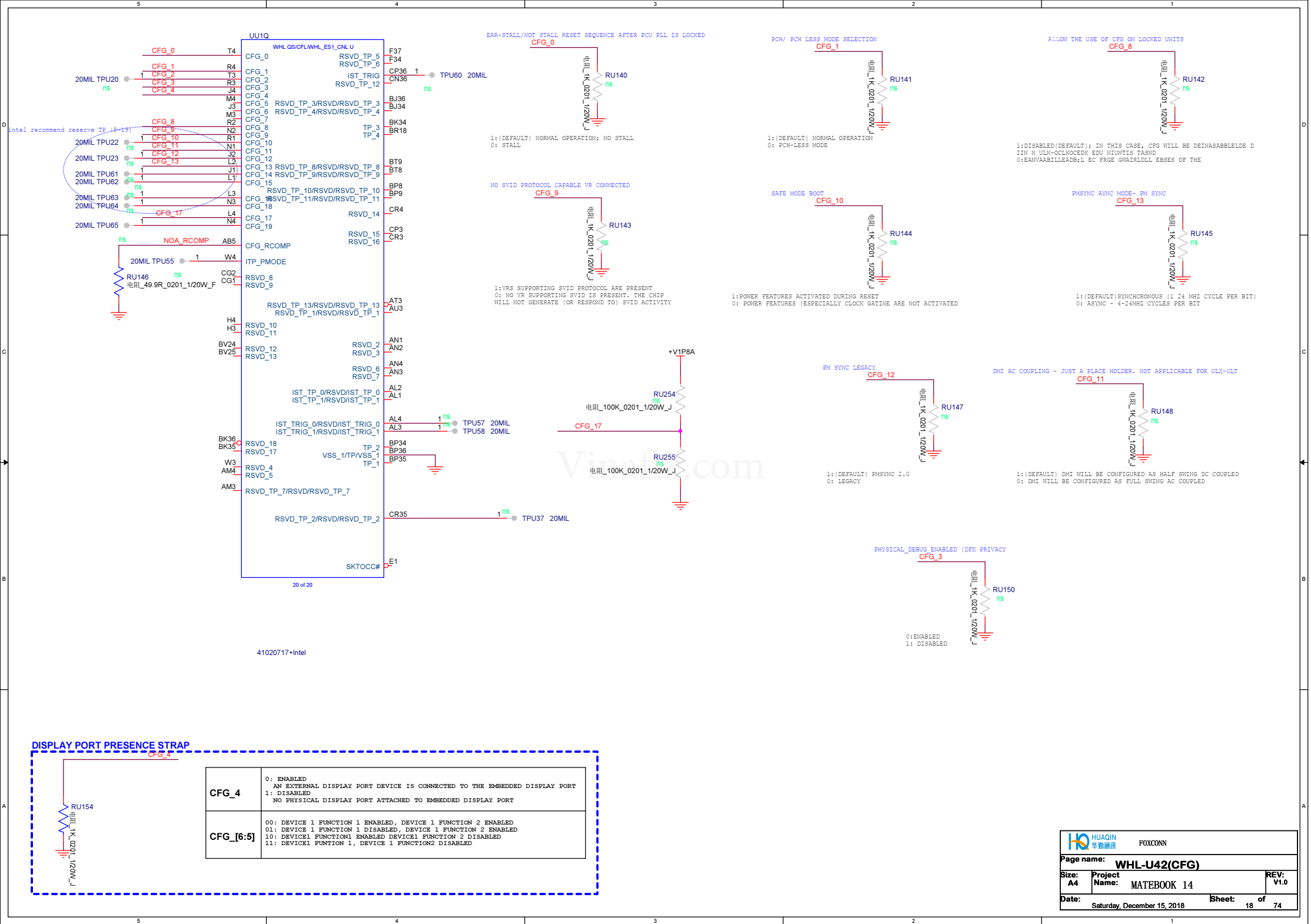
17 of 20
41020717+Intel



18 of 20
41020717+Intel

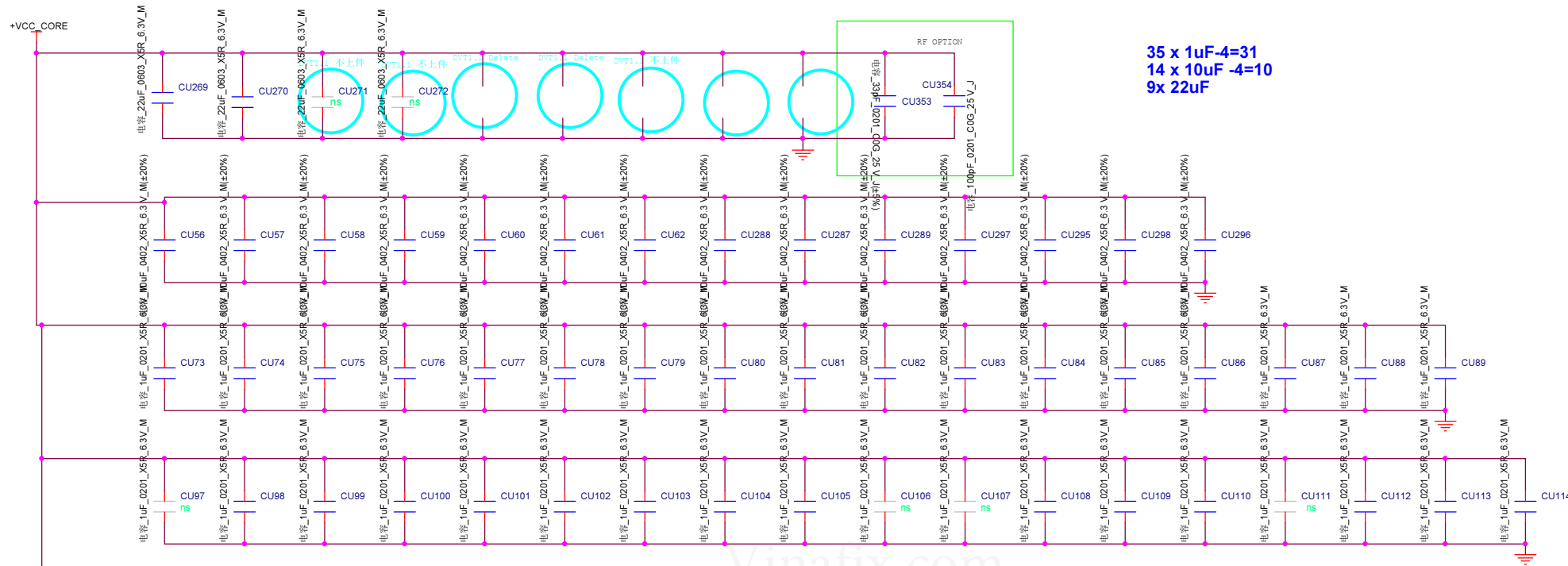


19 of 20
41020717+Intel

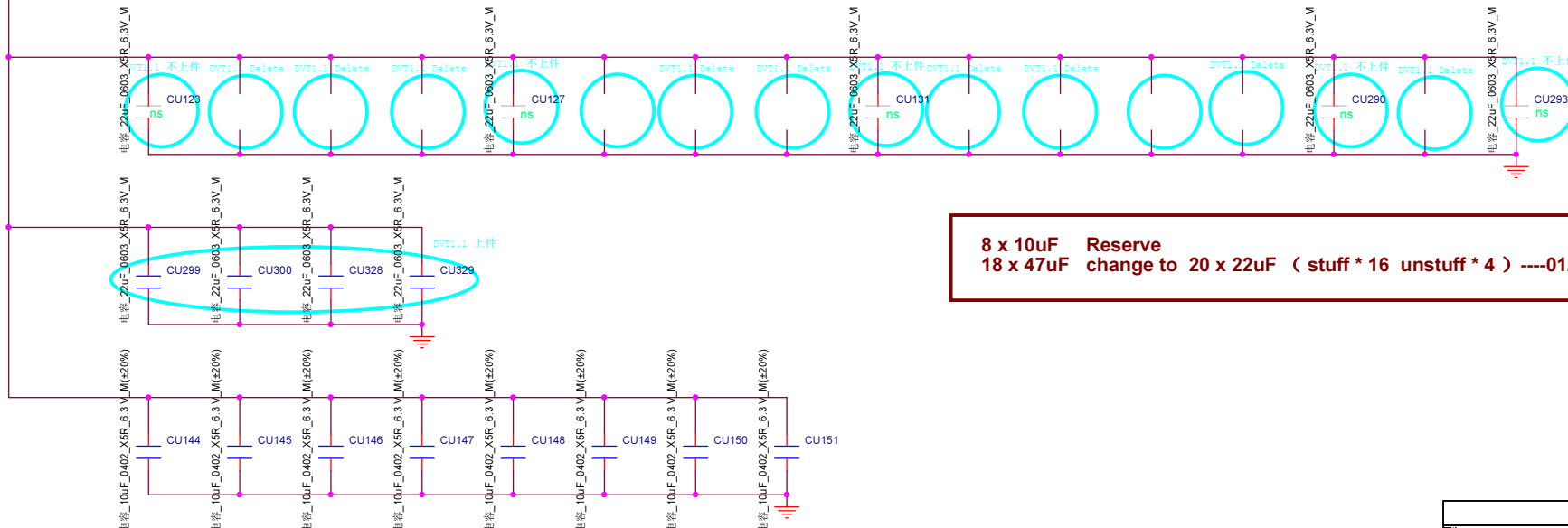


PLACE THESE CAPS UNDERNEATH BGA AREA

+VCCCORE



PLACE CLOSE TO PACKAGE ON PRIMARY SIDE



File	<Title>		
Size	Document Number	Rev	
A3	<Doc>	<Code>	
Date	Saturday, December 15, 2018	Sheet	19 of 74

[illegible]

PLACE CLOSE TO PACKAGE ON PRIMARY SIDE

15 x 22uF change to 16 x 22uF (stuff * 14 unstuff * 2)
8 x 47uF delete ----01/15

CU152 CU153 CU154 CU155 CU156 CU157 CU158 CU159 CU160 CU161 CU162

电容_22uF_0.003_X4R_6.3V_M

CU163 CU164 CU165 CU166 CU167

电容_22uF_0.003_X4R_6.3V_M

ns

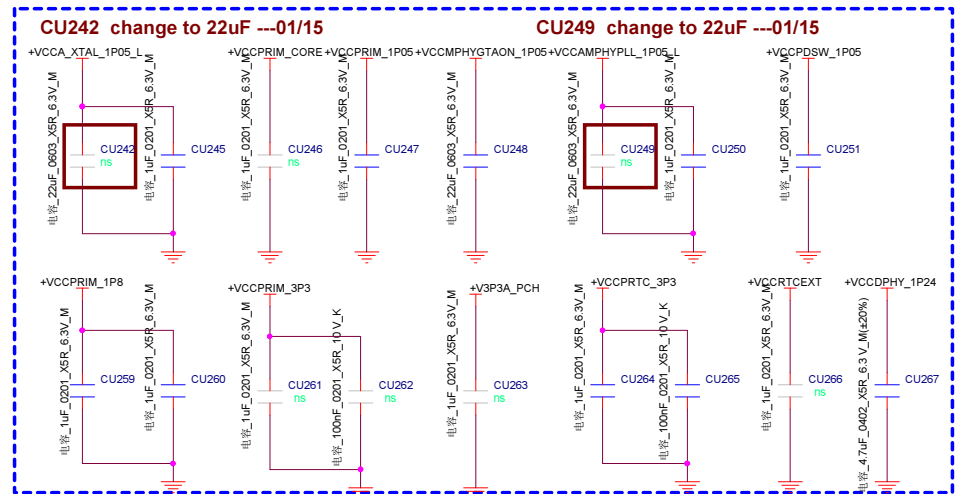
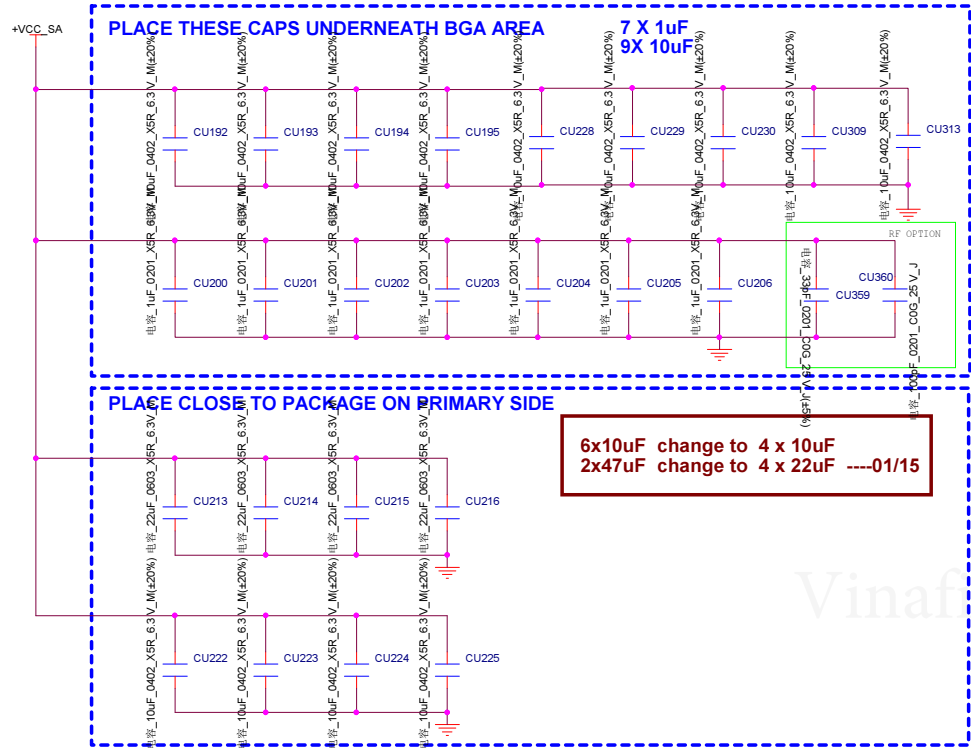
DVT改成不上件

DVT改成上件

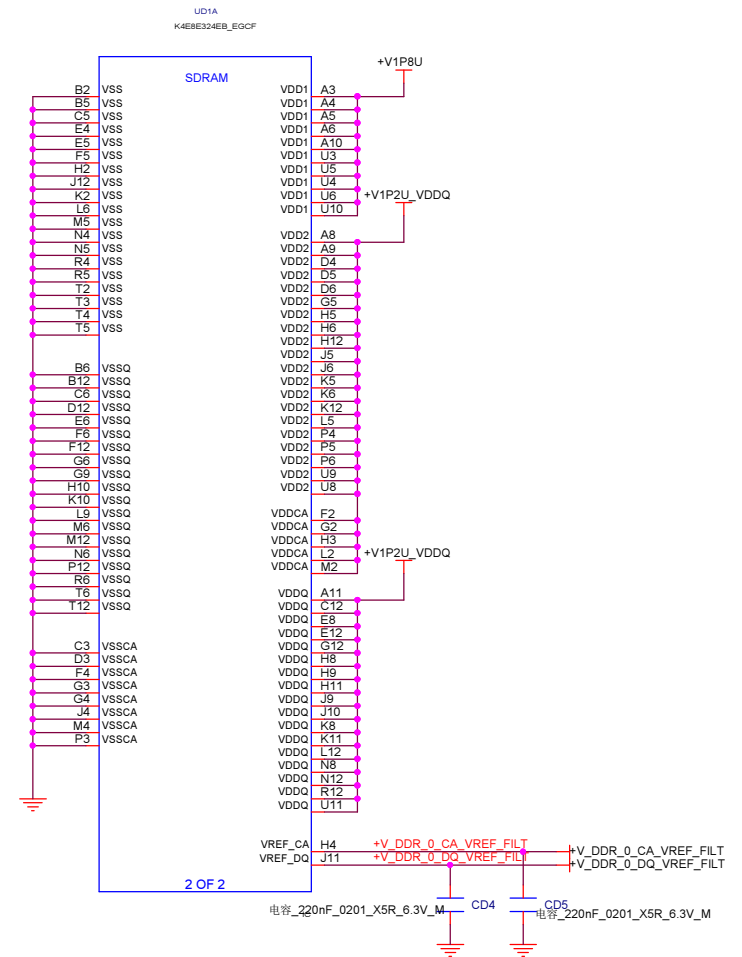
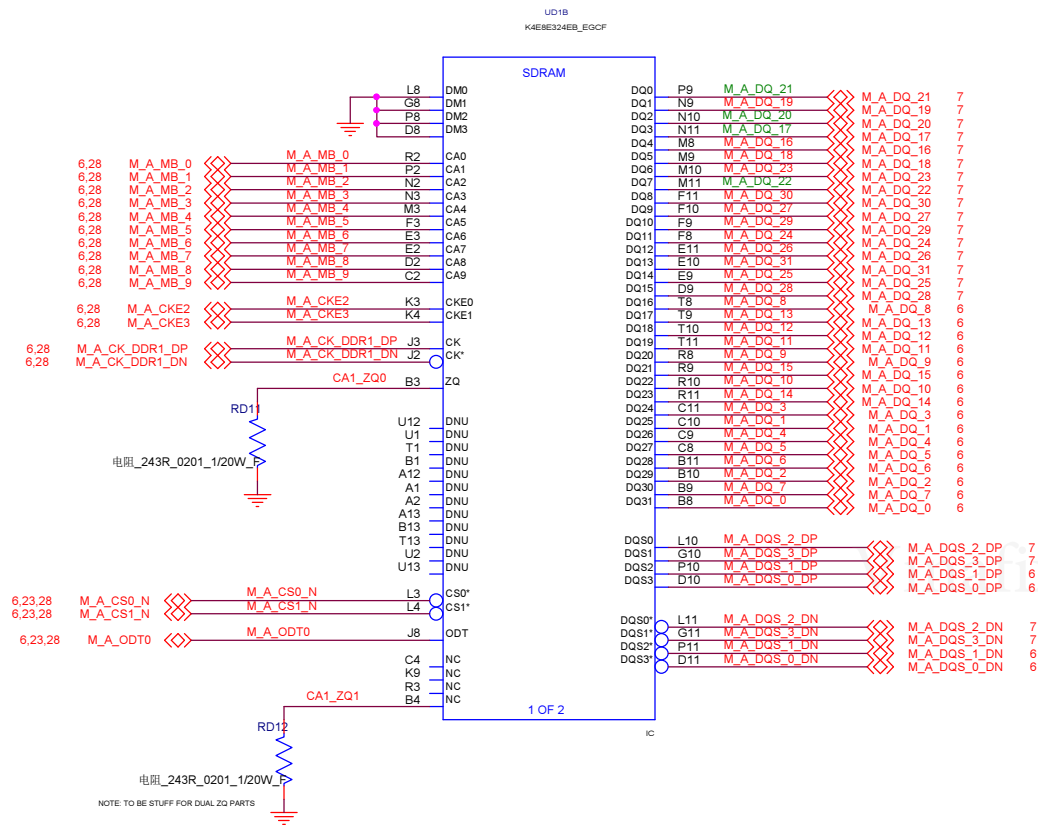
15 x 22uF change to 16 x 22uF (stuff * 14 unstuff * 2)
8 x 47uF delete ----01/15

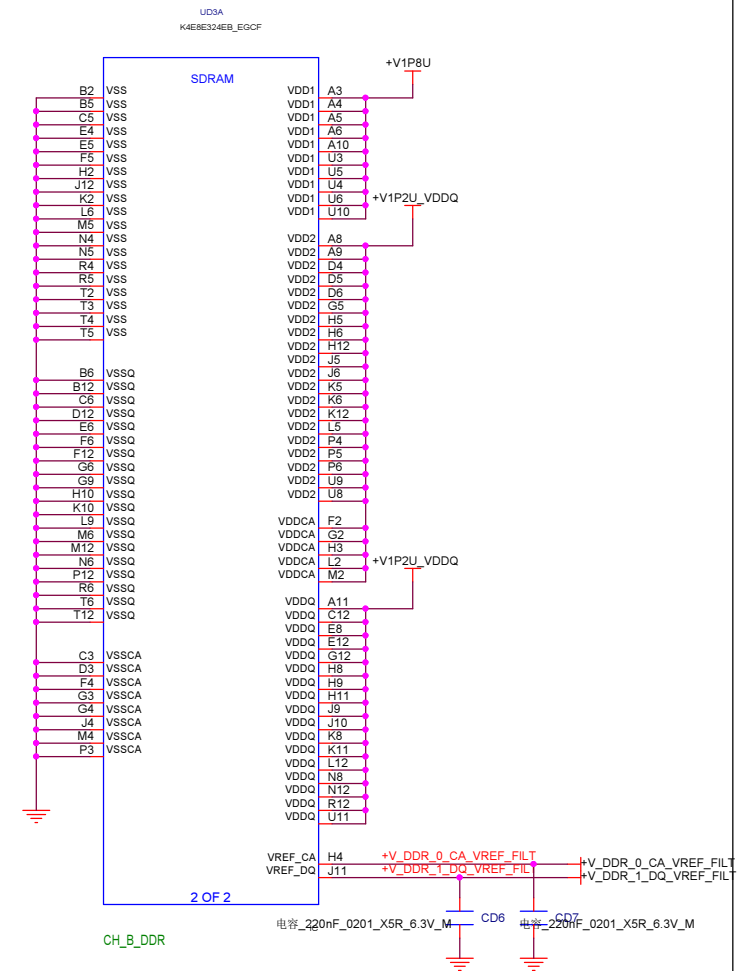
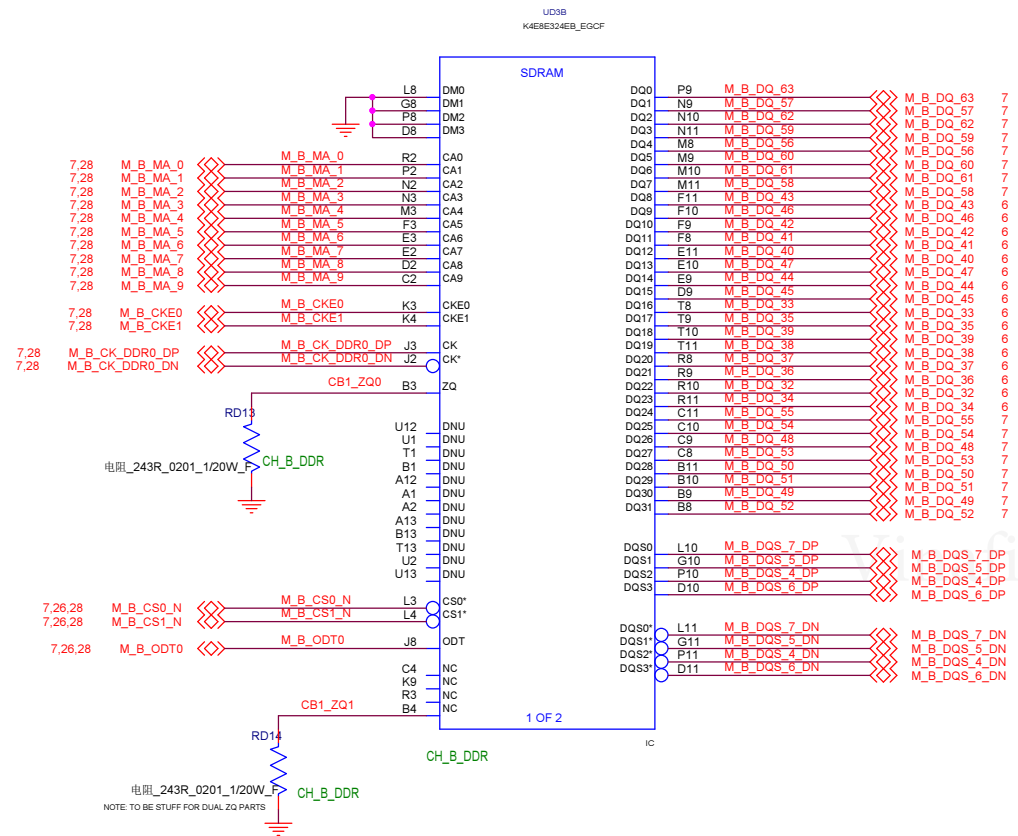
www.teknisi-indonesia.com

Title <Title>			
Size A3	Document Number <Doc>		Rev <RevCode>
Date:	Saturday, December 15, 2018	Sheet 20 of 74	

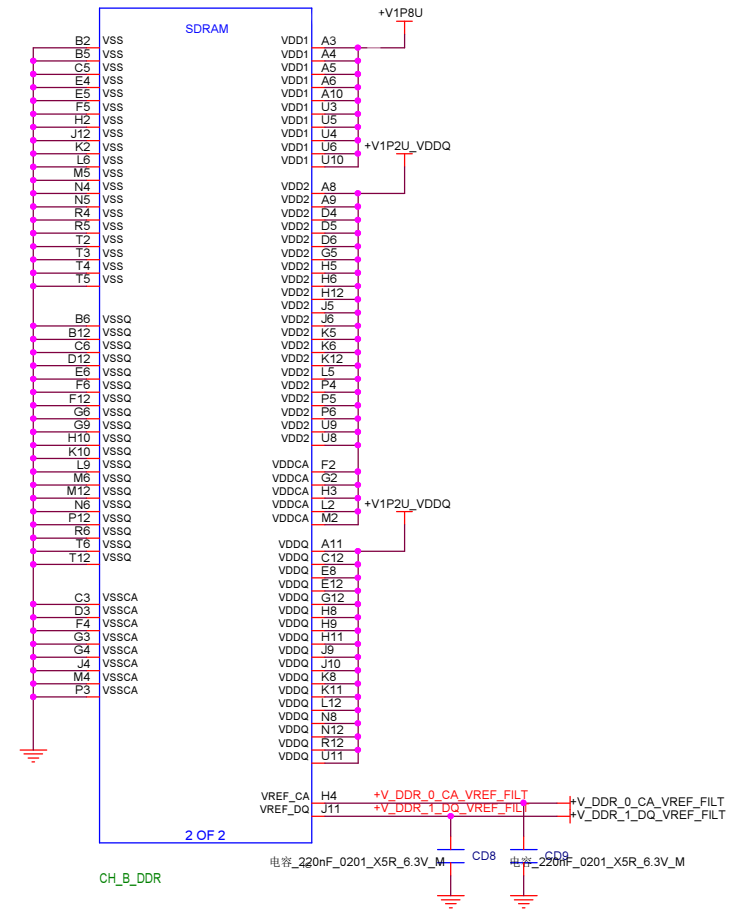
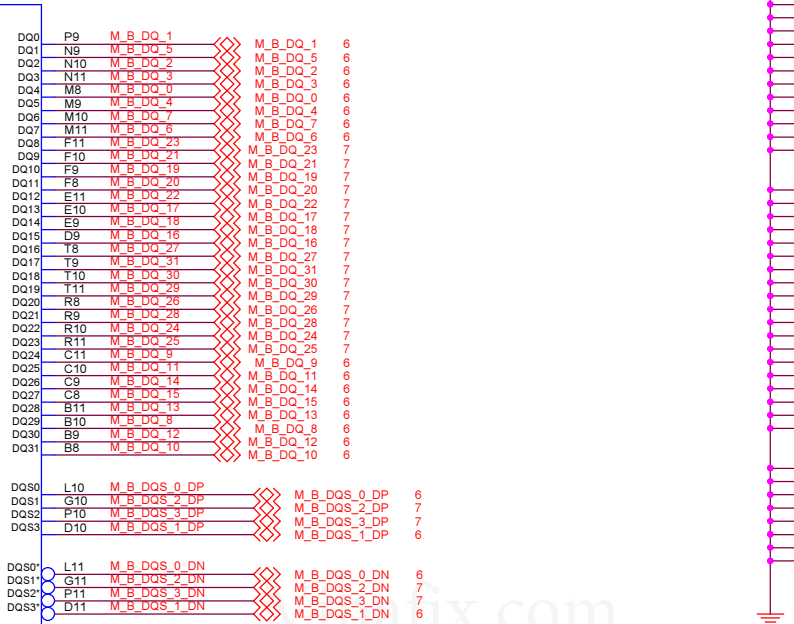
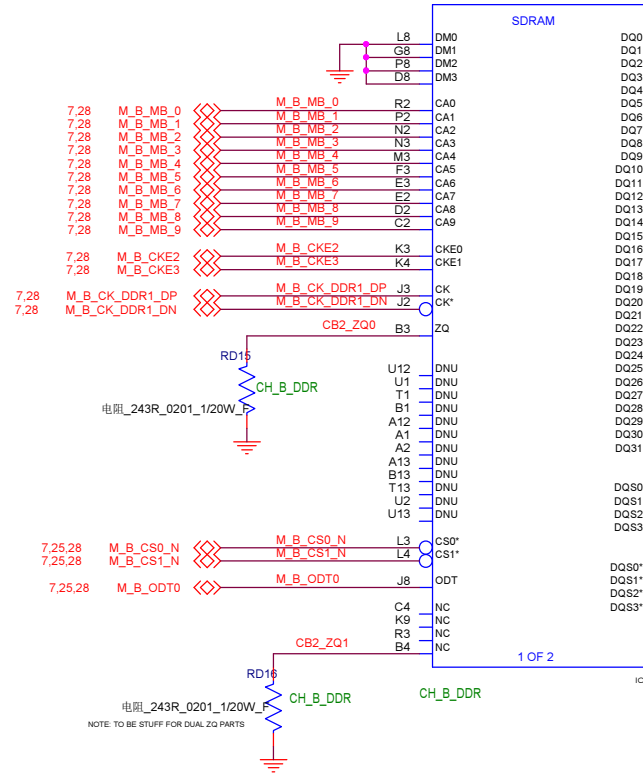


www.teknisi-indonesia.com



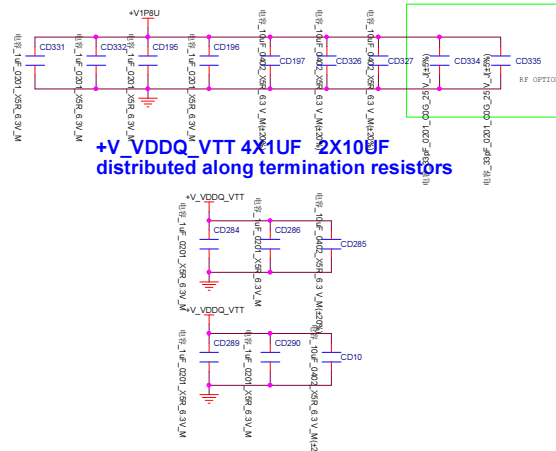
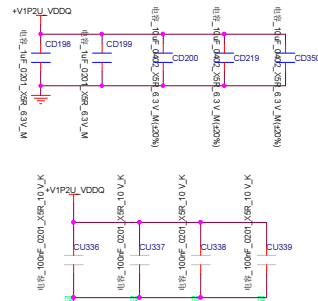
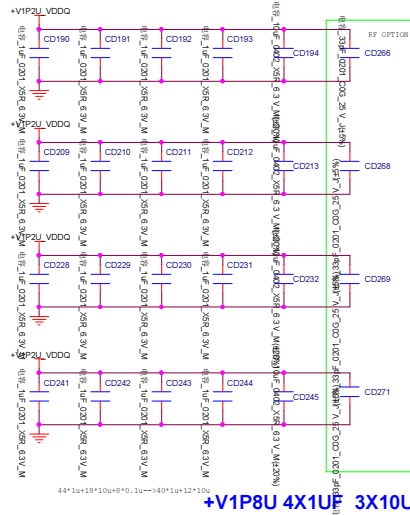


UD4B
K4E8E324EB_EGCF



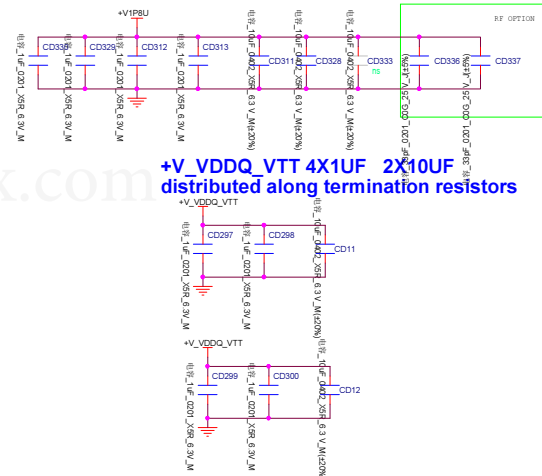
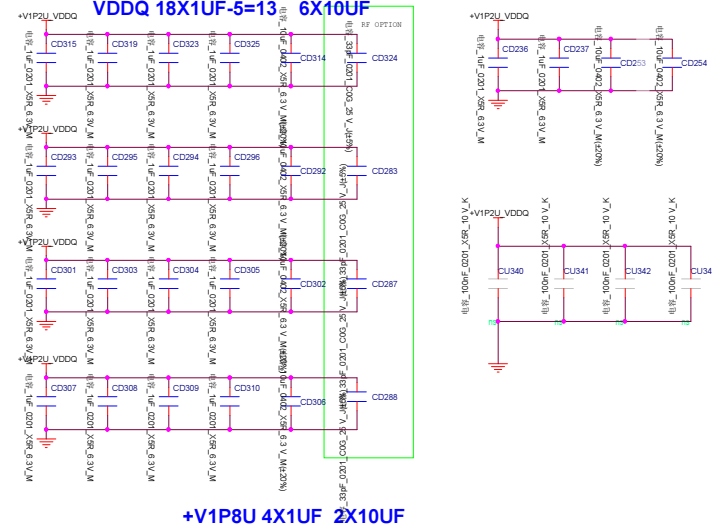
www.teknisi-indonesia.com

VDDQ 18X1UF-5=13 6X10UF+1=7

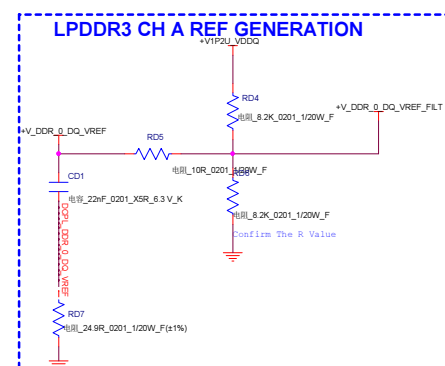
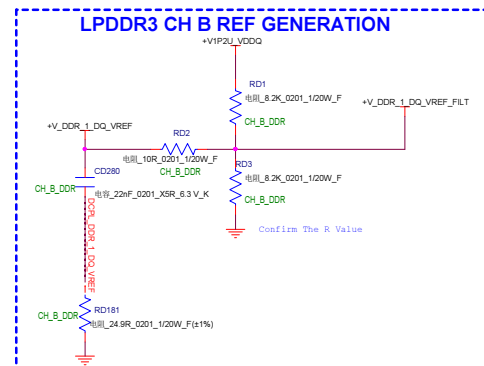
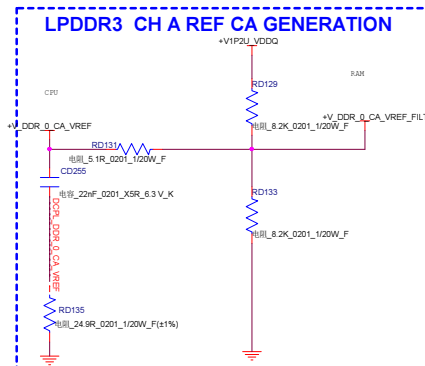


DECOUPLING CAPACITORS FOR DDR CHANNEL B

VDDQ 18X1UF-5=13 6X10UF



All caps need to put to DRAM as close as possible.



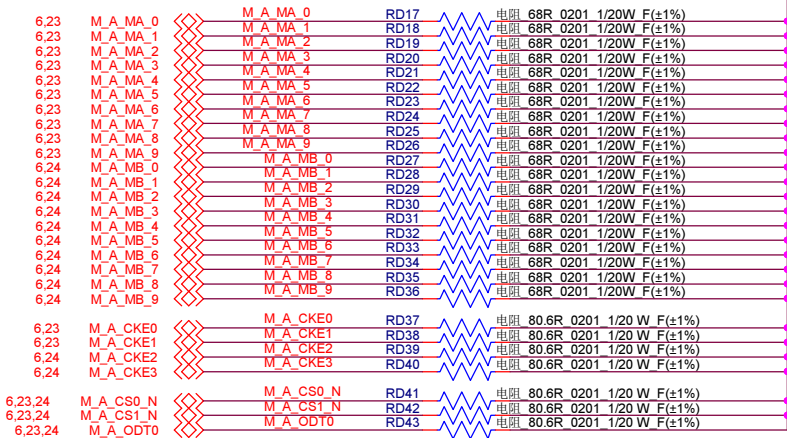
MEMORY TERMINATIONS

CHANNEL A

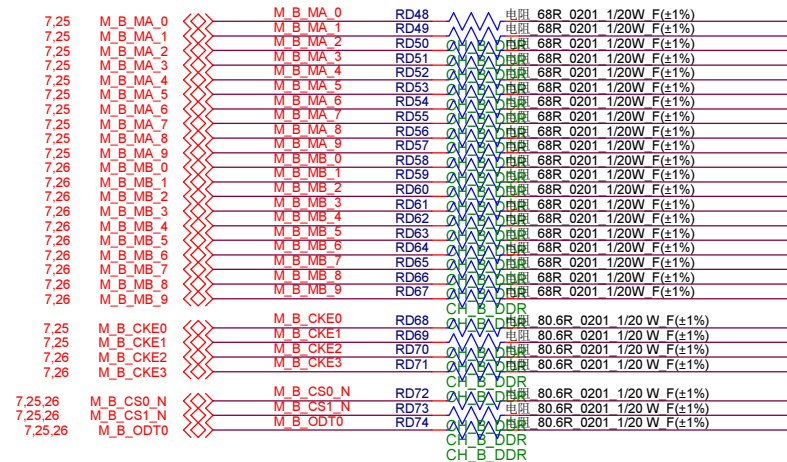
MEMORY TERMINATIONS

CHANNEL B

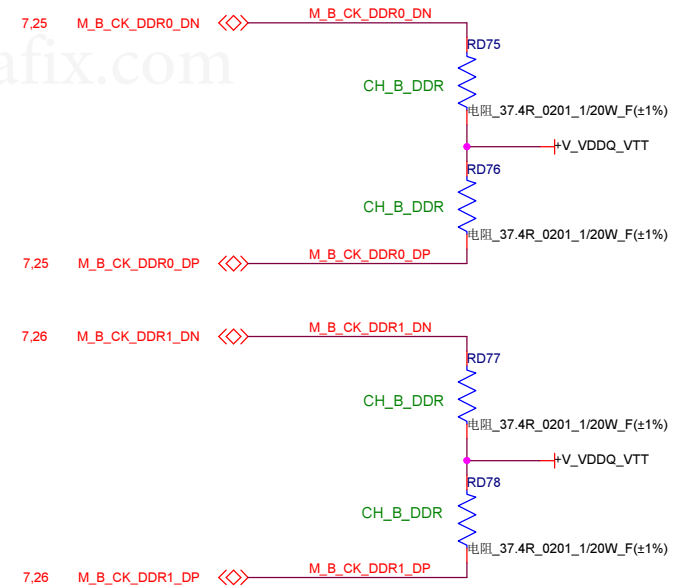
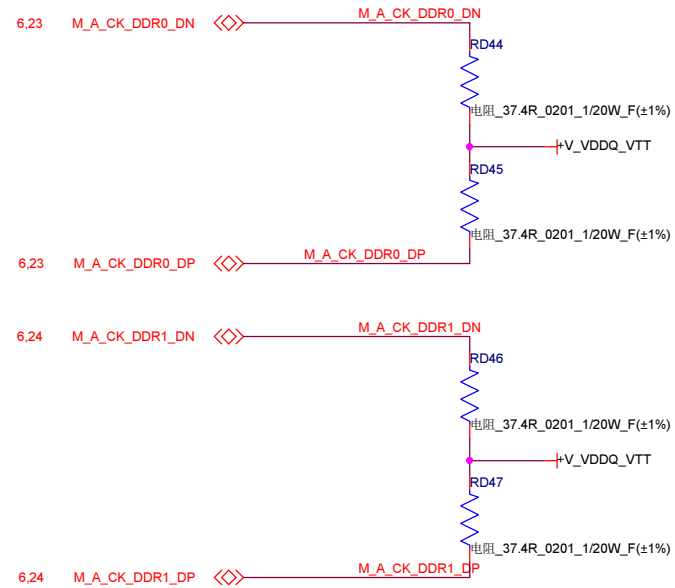
+V_VDDQ_VTT

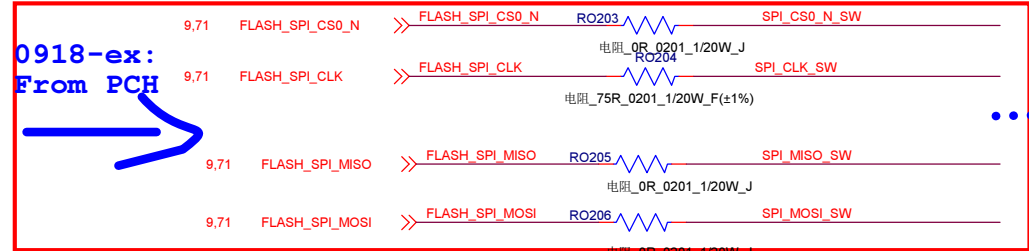
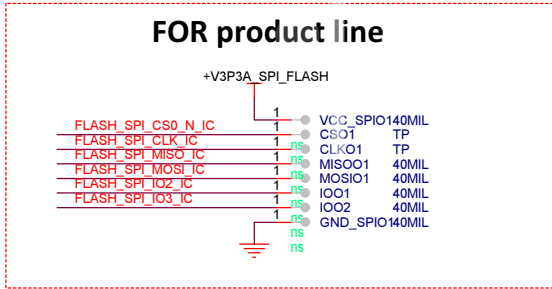
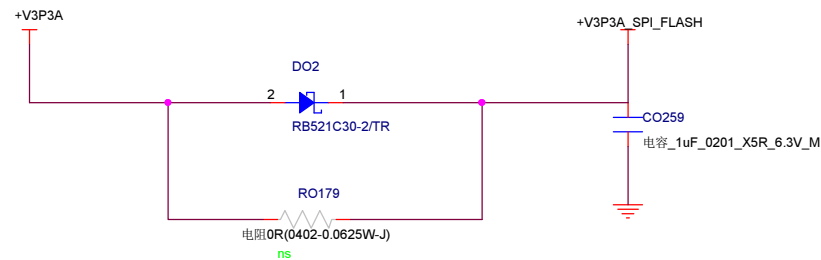


+V_VDDQ_VTT




Vinafix.com



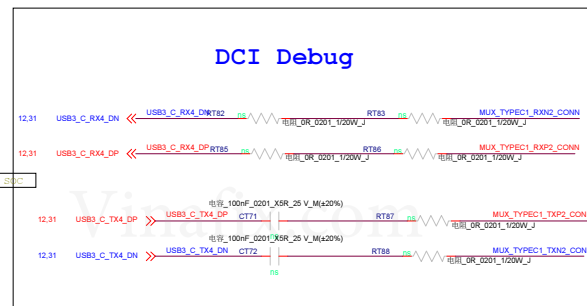
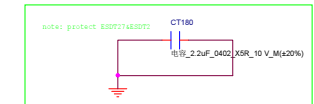
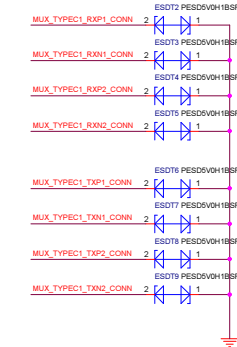
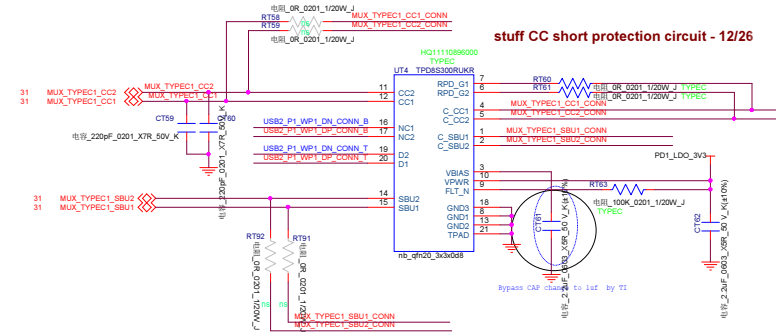
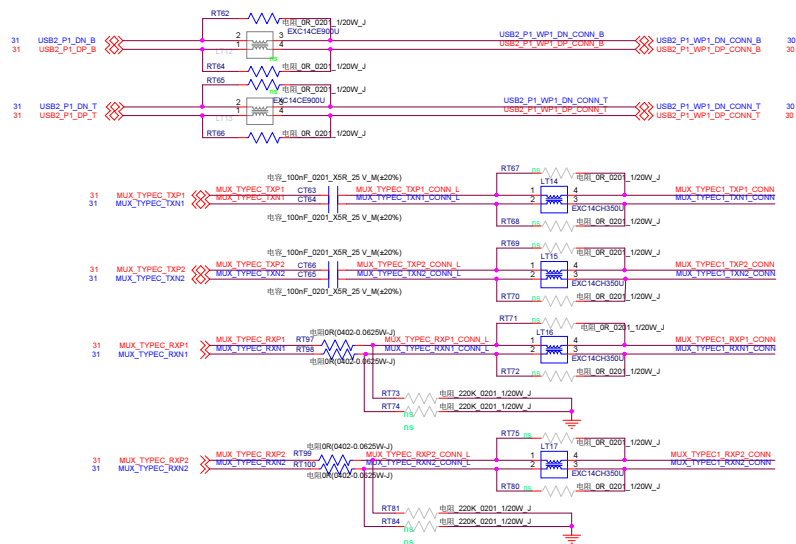


0916-ex:
by pass by 0 ohm resistors



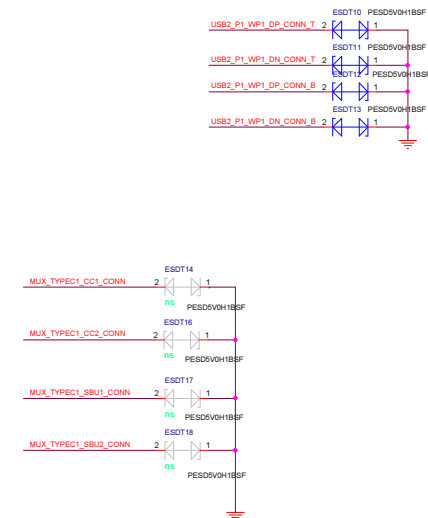
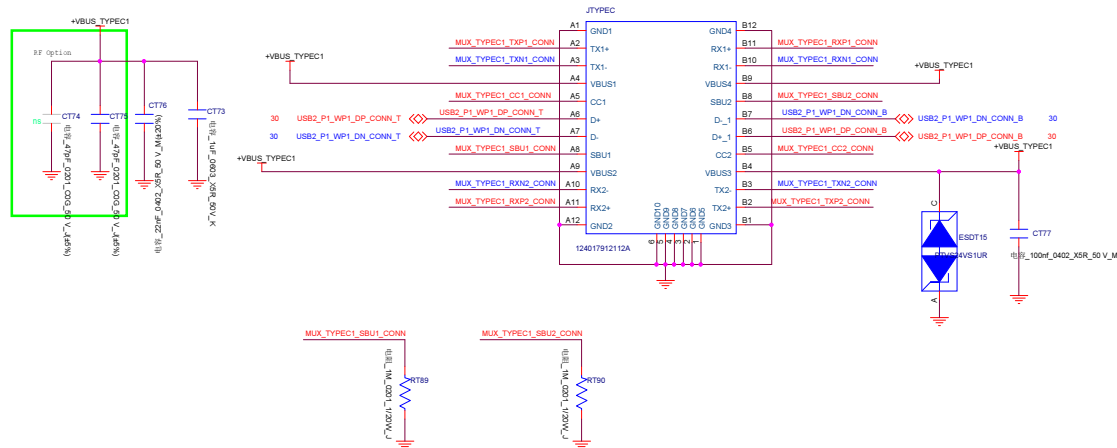
 HUAQIN 华勤通讯		FOXCONN	
Page name: SYSTEM FLASH			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 29	of 74	

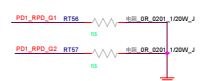
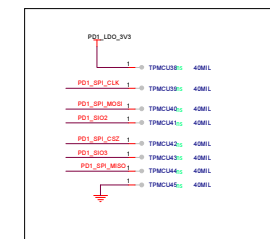
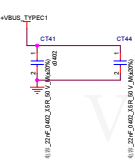
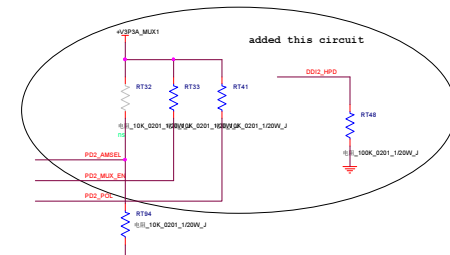
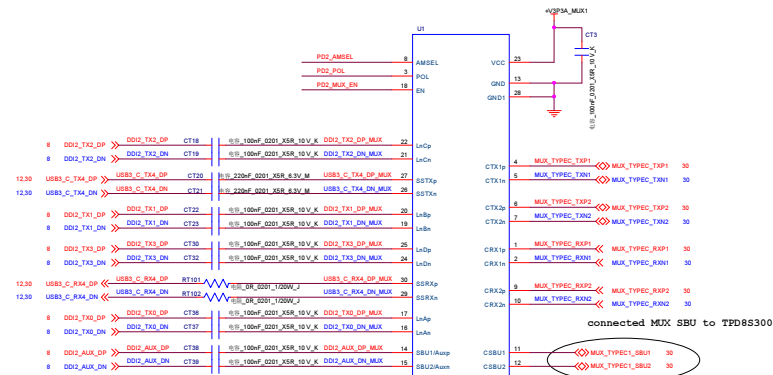
chang the C(and R) and CMC
relative location



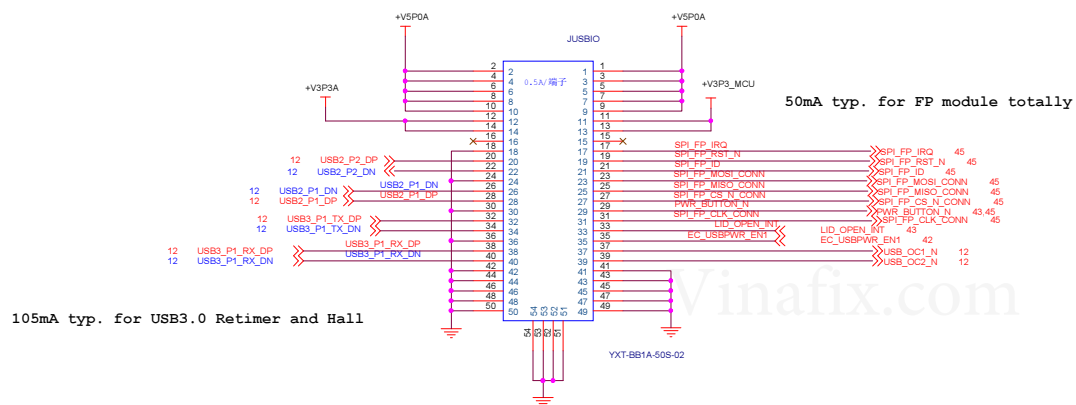
output to SOC	
---------------	--

0606---与龙专确认 EMC 型号OK, 料号待确认OK

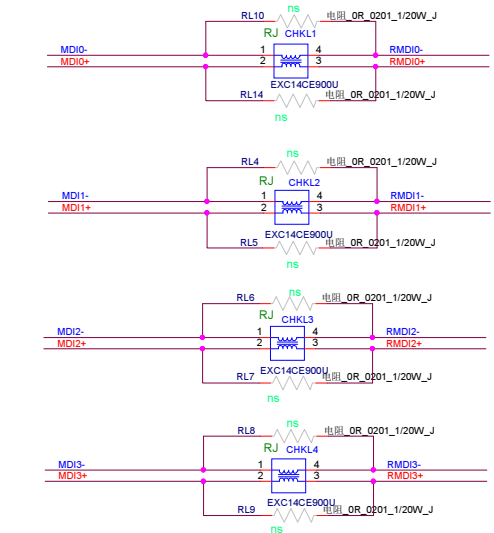
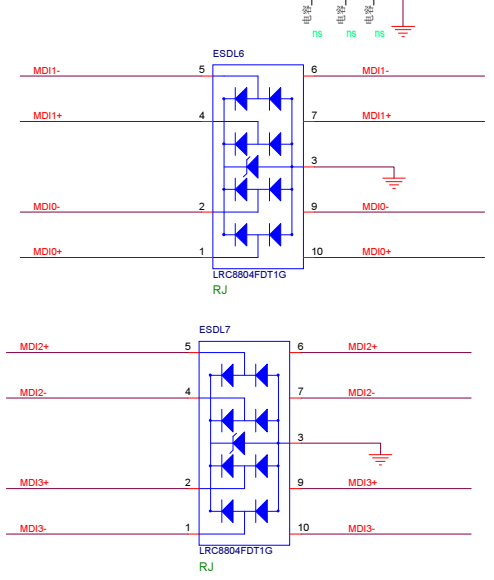
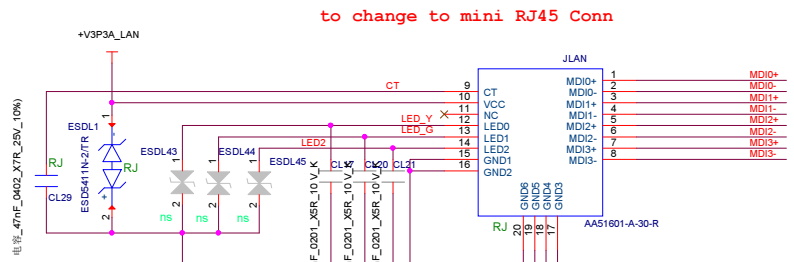


[illegible]

changed to PD_GPIO5 and ns RT292



www.teknisi-indonesia.com

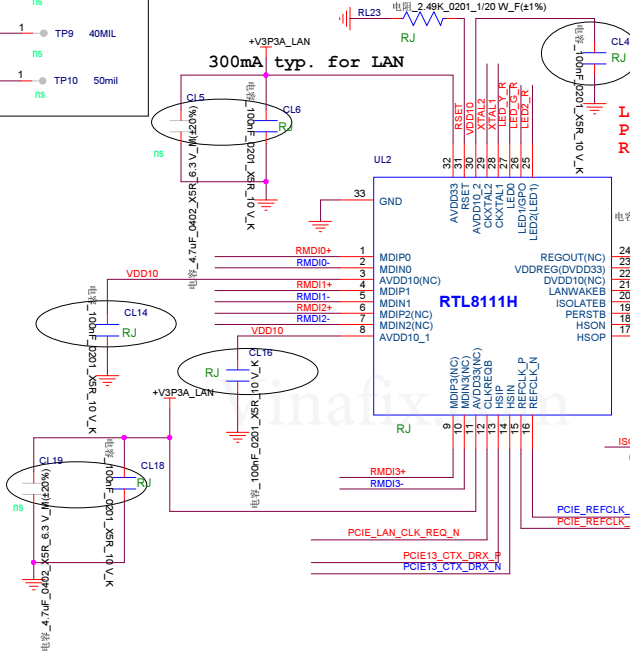


to change to mini RJ45 Conn

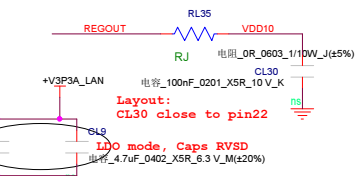
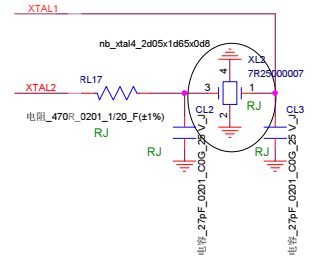
11/05: For Factory Test
Layout: TP must close to
Mini-RJ45 connector JLAN

R9 value should be
2.49K (1%)
for all application.

300mA typ. for LAN



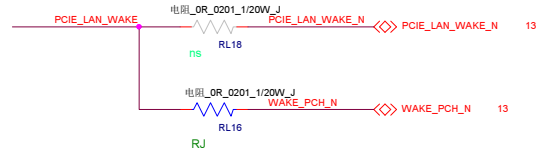
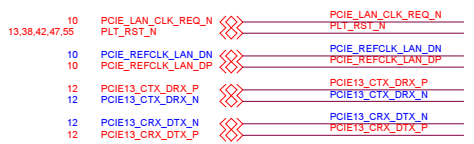
Layout:
Power trace VDDREG > 40 mil,
REGOUT trace > 60 mil




Layout Guide for PWR(all within 200mils):

- 1, pin24--CL10 (0.1uF)
- 2, For VDD33 (pin11, pin32, pin23)
(1), pin11--CL18 (0.1uF) and CL19 (RVSD, 4.7uF)
(2), pin32--CL6 (0.1uF) and CL5 (RVSD, 4.7uF)
(3), pin23--CL8 (0.1uF) and CL9 (RVSD, 4.7uF)
- 3, For VDD10 (pin3, pin8, pin22, pin30)
(1), pin3--CL14 (0.1uF)
(2), pin8--CL16 (0.1uF)
(3), pin22--CL12 (0.1uF) and CL11 (RVSD, 1uF)
(4), pin30--CL4 (0.1uF)

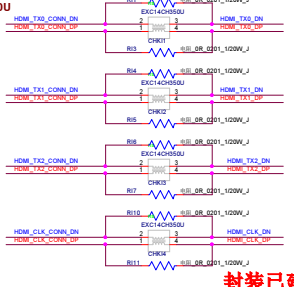
300mA typ. for LAN



Vinafix.com

 HUAQIN 华勤通讯		FOXCONN	
Page name: BLANK			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018		Sheet: 34	of 74

0201 1/2066 J



place close almost

place close almost



封装已建
申请料号



DDI1_TX0_ON	DDI1_TX0_ON	8
DDI1_TX0_DP	DDI1_TX0_DP	8
DDI1_TX1_ON	DDI1_TX1_ON	8
DDI1_TX1_DP	DDI1_TX1_DP	8
DDI1_TX2_ON	DDI1_TX2_ON	8
DDI1_TX2_DP	DDI1_TX2_DP	8
DDI1_TX3_ON	DDI1_TX3_ON	8
DDI1_TX3_DP	DDI1_TX3_DP	8

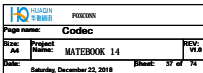


DDI1_TX0_ON	DDI1_TX0_ON	8
DDI1_TX0_DP	DDI1_TX0_DP	8
DDI1_TX1_ON	DDI1_TX1_ON	8
DDI1_TX1_DP	DDI1_TX1_DP	8
DDI1_TX2_ON	DDI1_TX2_ON	8
DDI1_TX2_DP	DDI1_TX2_DP	8
DDI1_TX3_ON	DDI1_TX3_ON	8
DDI1_TX3_DP	DDI1_TX3_DP	8

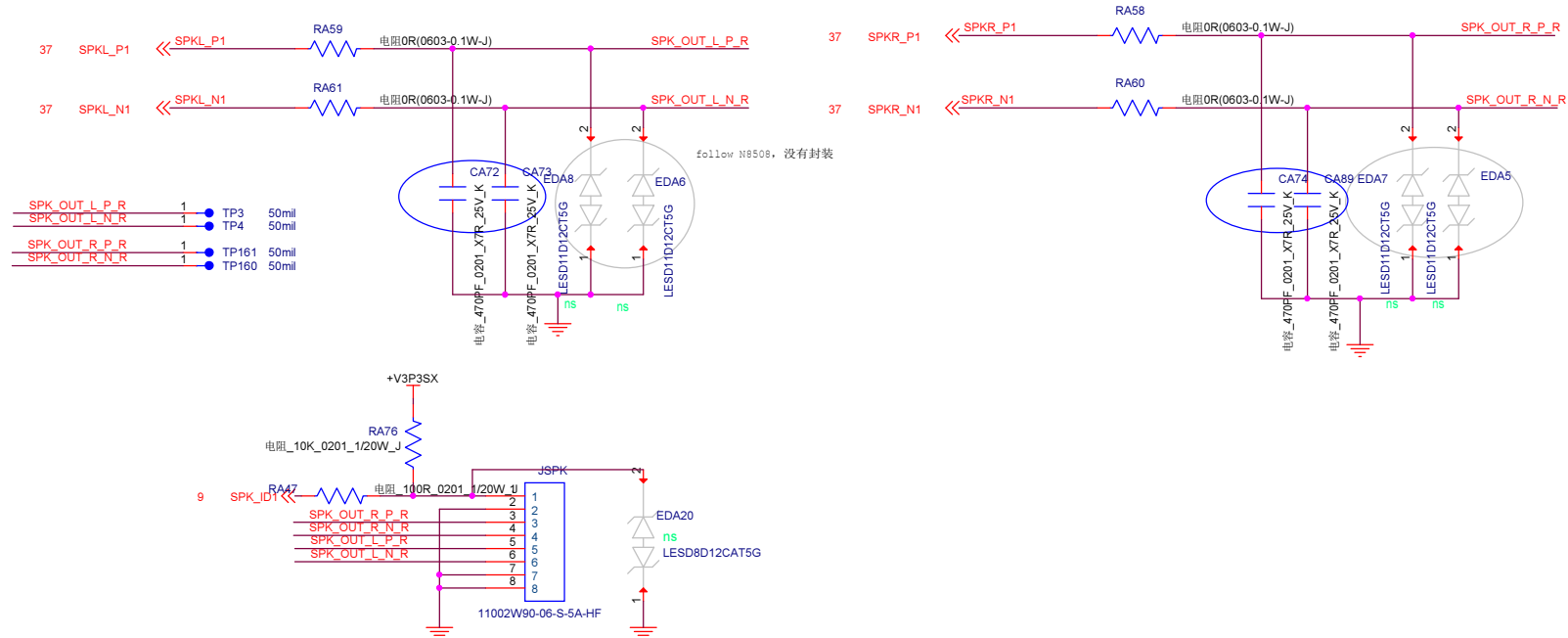


FOR product line

Signal	Pin	TP	Value
DMIC_CLK1_CORIN	1	TP142	50mV
DMIC_DATA1_CORIN	1	TP141	50mV
DMIC_CLK2_CORIN	1	TP185	50mV
DMIC_DATA2_CORIN	1	TP140	50mV
DMIC_CLK3_CORIN	1	TP143	50mV
DMIC_DATA3_CORIN	1	TP157	50mV

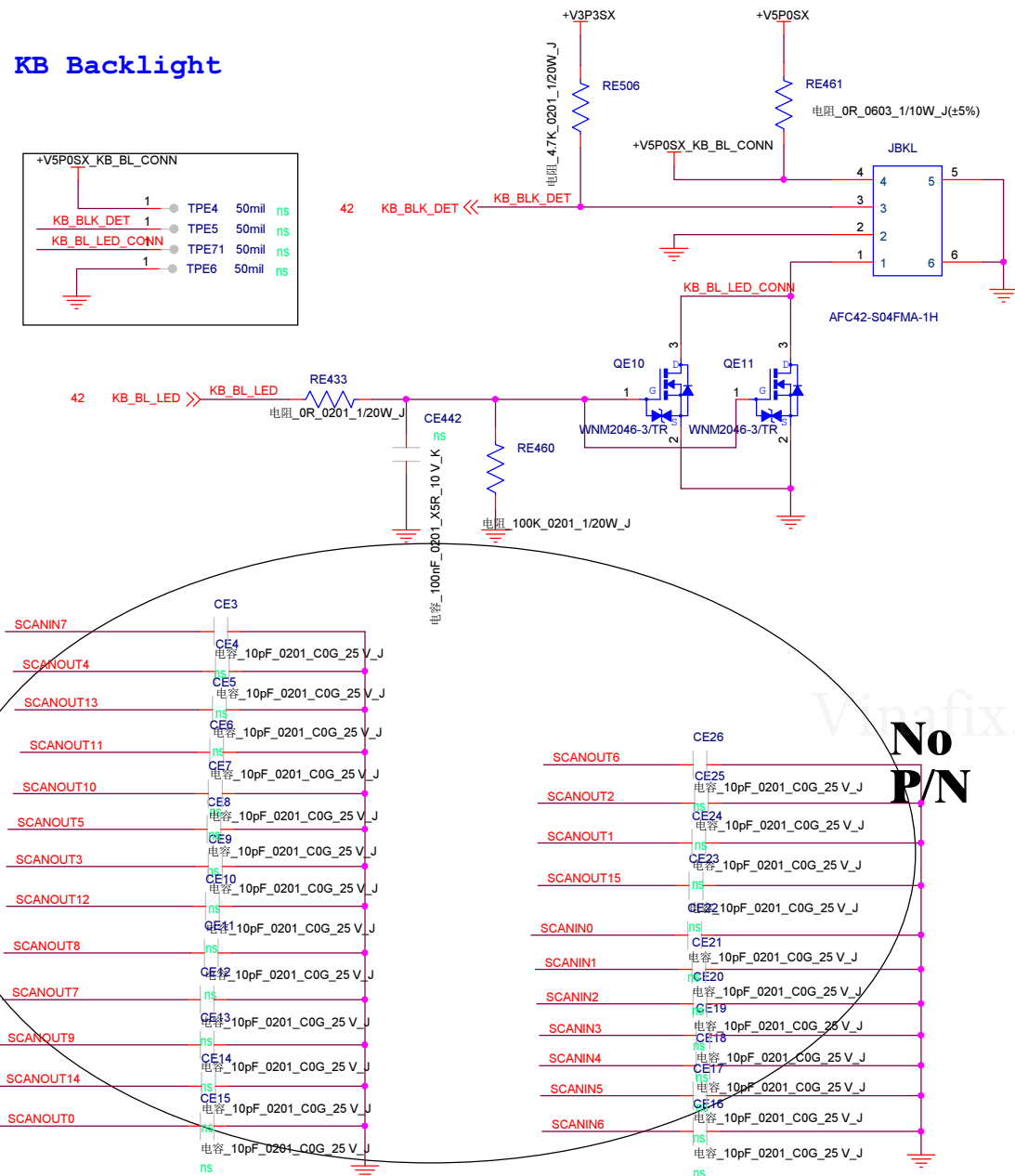


www.teknisi-indonesia.com



+V5P0SX_KB_BL_CONN

Signal	Pin	Distance	Timing
KB_BLK_DET	1	50mil	ns
KB_BLK_DET	1	50mil	ns
KB_BL_LED_CONN		50mil	ns
1		50mil	ns

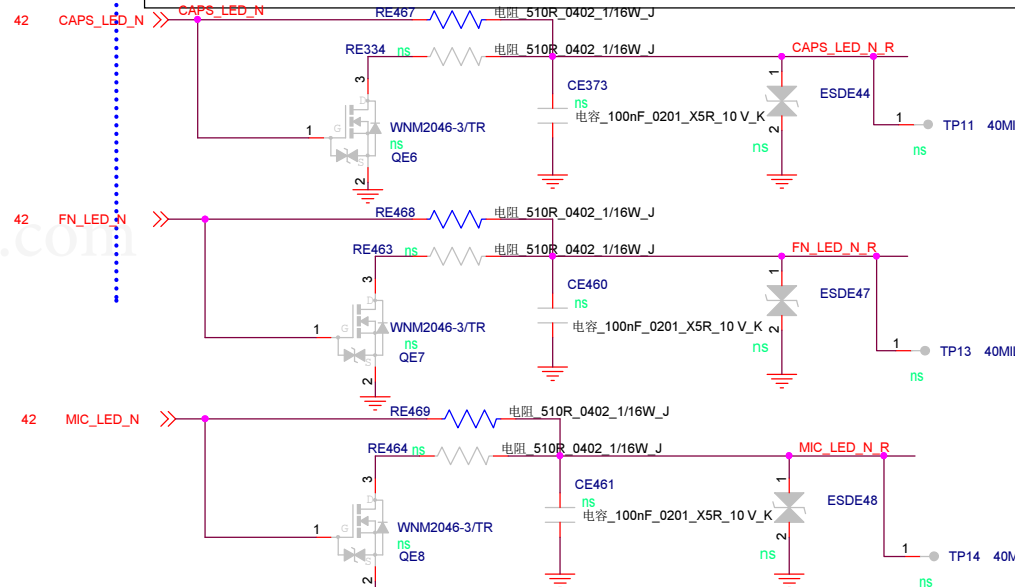


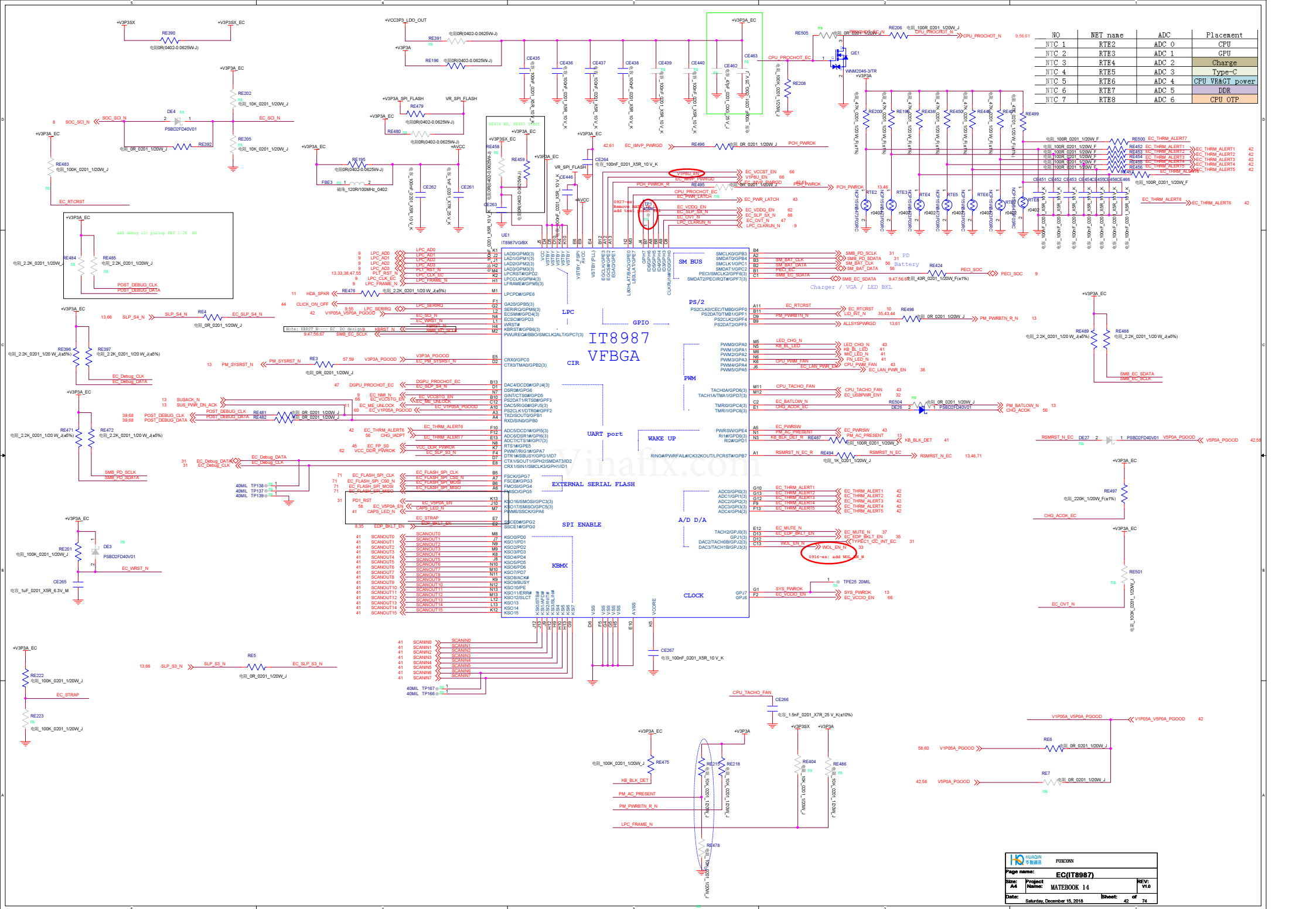
KB_CONN

KB_CONN Pin	Signal	JKB Pin
42	SCANIN0	1
42	SCANIN1	2
42	SCANIN2	3
42	SCANIN3	4
42	SCANIN4	5
42	SCANIN5	6
42	SCANIN6	7
42	SCANIN7	8
42	SCANOUT4	9
42	SCANOUT13	10
42	SCANOUT11	11
42	SCANOUT10	12
42	SCANOUT5	13
42	SCANOUT3	14
42	SCANOUT12	15
42	SCANOUT8	16
42	SCANOUT7	17
42	SCANOUT9	18
42	SCANOUT14	19
42	SCANOUT0	20
42	SCANOUT6	21
42	SCANOUT2	22
42	SCANOUT1	23
42	SCANOUT15	24
	FN_LED_N_R	25
	CAPS_LED_N_R	26
	MIC_LED_N_R	27
		28
		29
		30

Physical Layout:

- Power:** +V5P0SX connected to pin 1 (TP12, 50mil).
- Capacitor:** CE2 (1uF, 0201_X5R_10 V_M(±20%)) connected to +V5P0SX and GND0.
- Crystal:** 4055w90-30-3pn-shl0atbr connected to pins 31 (GND0) and 32 (GND1).
- LEDs:** FN_LED_N_R, CAPS_LED_N_R, and MIC_LED_N_R connected to pins 25, 26, and 27 respectively.





NO	NET name	ADC	Placement
NTC 1	RTE1	ADC 0	CPU
NTC 2	RTE2	ADC 1	CPU
NTC 3	RTE3	ADC 2	Charge
NTC 4	RTE4	ADC 3	Type-C
NTC 5	RTE5	ADC 4	CPU VRAGT power
NTC 6	RTE6	ADC 5	DDR
NTC 7	RTE7	ADC 6	CPU OTP

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

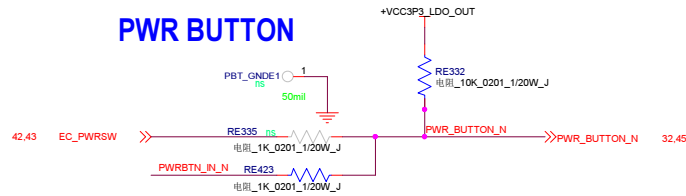
EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

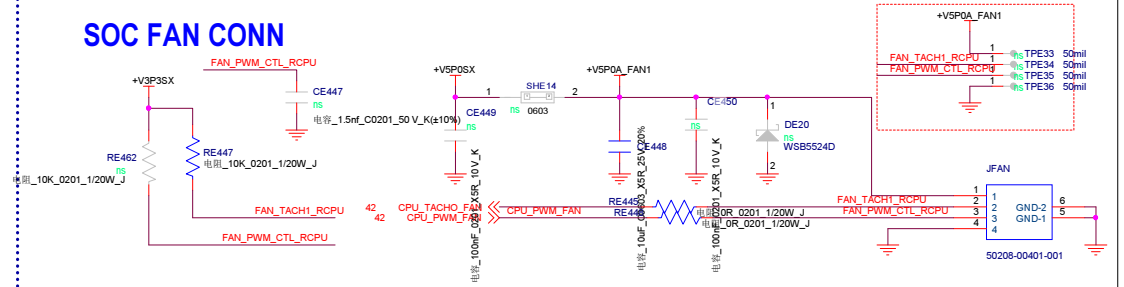
EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

EC_THRM_ALERT1	EC_THRM_ALERT1
EC_THRM_ALERT2	EC_THRM_ALERT2
EC_THRM_ALERT3	EC_THRM_ALERT3
EC_THRM_ALERT4	EC_THRM_ALERT4
EC_THRM_ALERT5	EC_THRM_ALERT5
EC_THRM_ALERT6	EC_THRM_ALERT6
EC_THRM_ALERT7	EC_THRM_ALERT7

PWR BUTTON

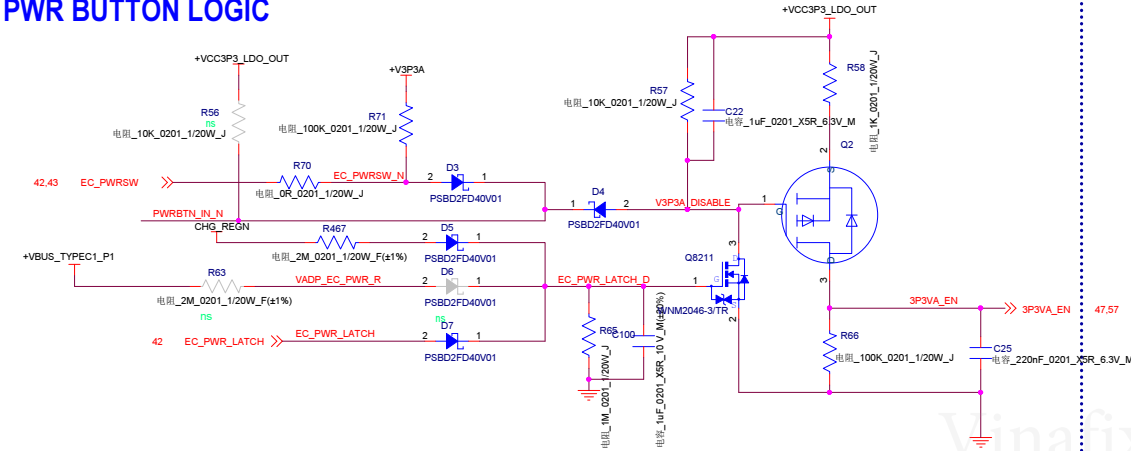


SOC FAN CONN

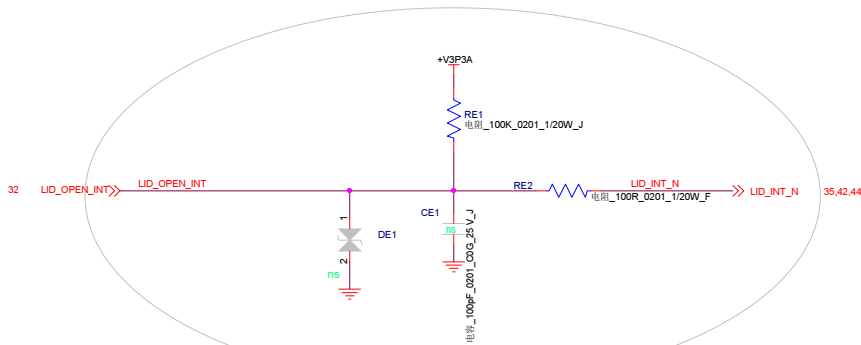


FOR product line

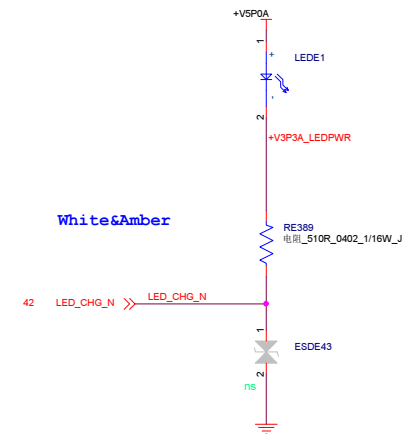
PWR BUTTON LOGIC




HALL

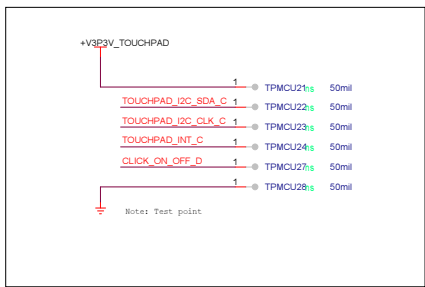
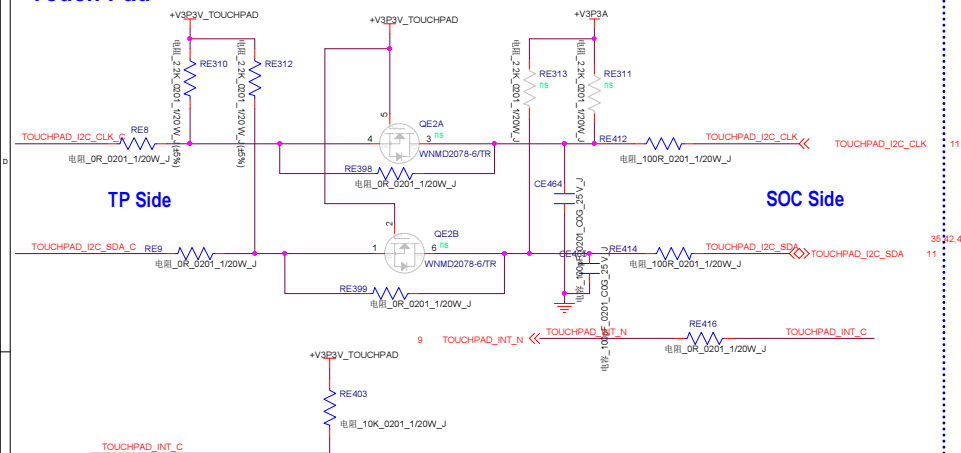


LED



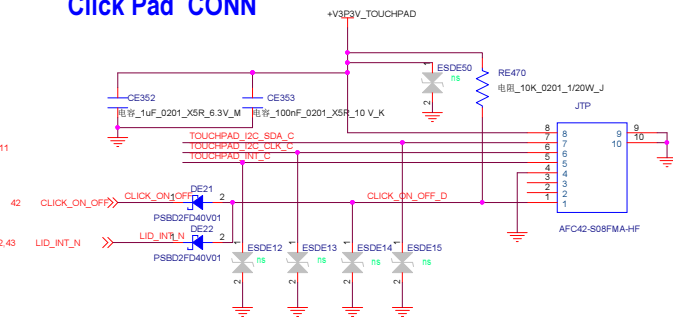
 HUAQIN 华勤通信		FOXCONN	
Page name: BUTTON/FAN/LED/Hall			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 43	of 74	

Touch Pad




Click Pad CONN

PIN1对Pin1



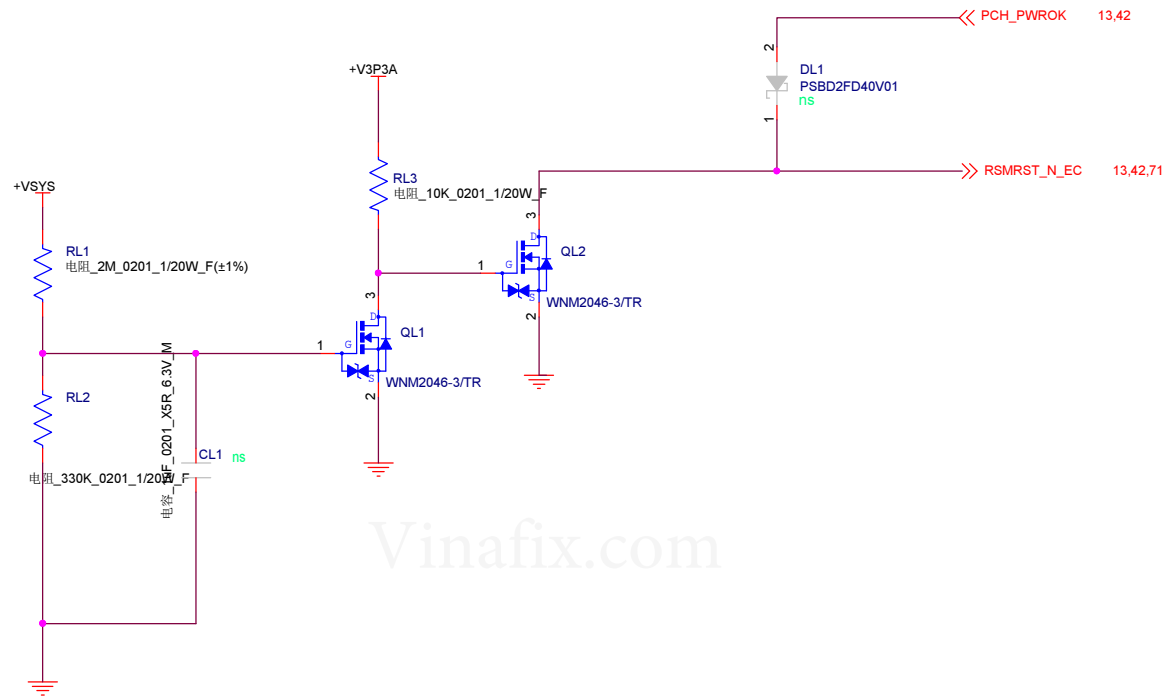
Vinafix.com

 HUAQIN 华勤通信		FOXCONN	
Page name: TouchPad			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 44	of 74	


www.teknisi-indonesia.com

Vinafix.com

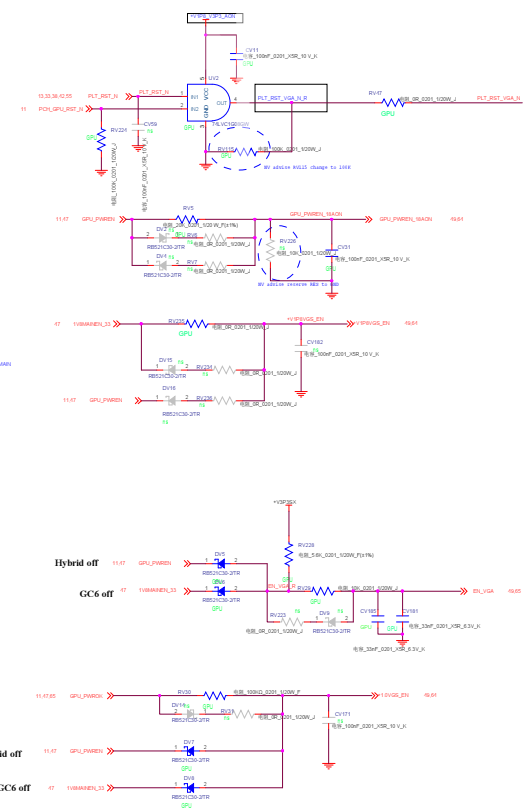
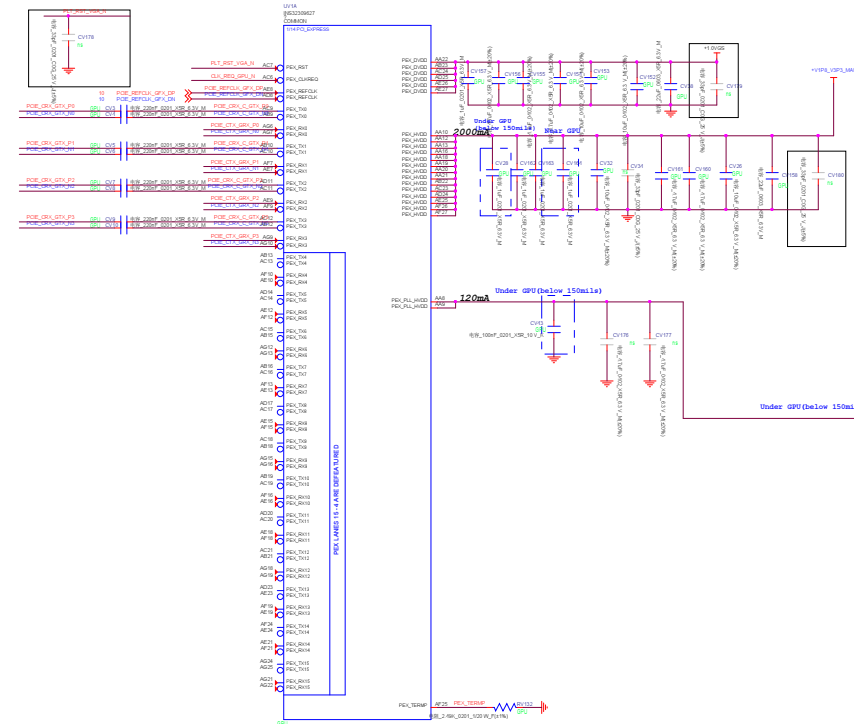
Finger Print CONN



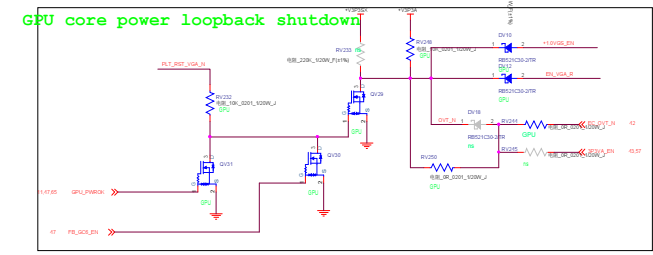
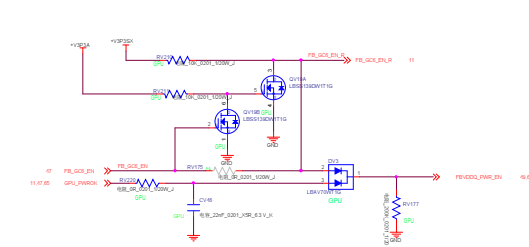
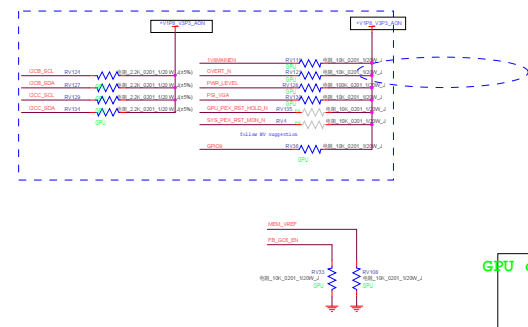
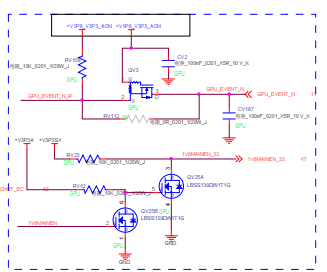
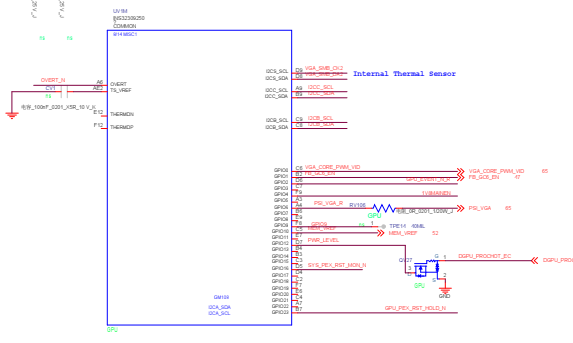
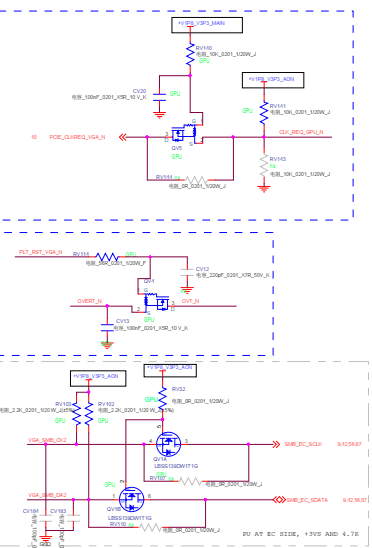
Vinafix.com

 HUAQIN 华勤通讯		FOXCONN	
Page name: BLANK			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 46		of 74

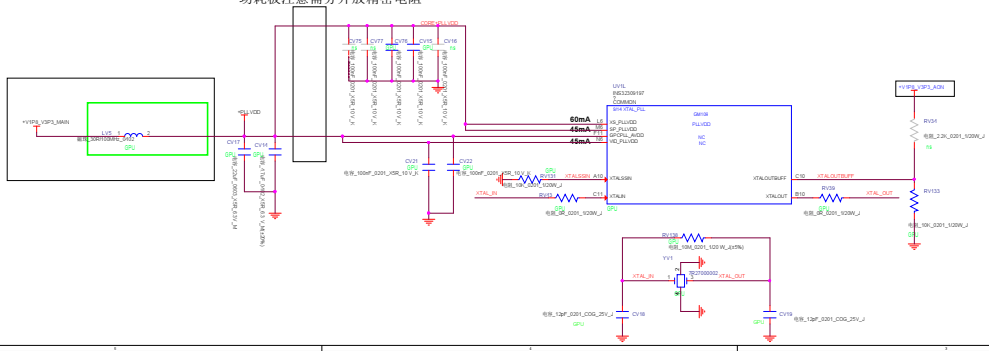
- 12 PDE_CSTX_CLK_0-3
- 12 PDE_CSTX_CLK_0-3
- 12 PDE_CSTX_CLK_0-3
- 12 PDE_CSTX_CLK_0-3

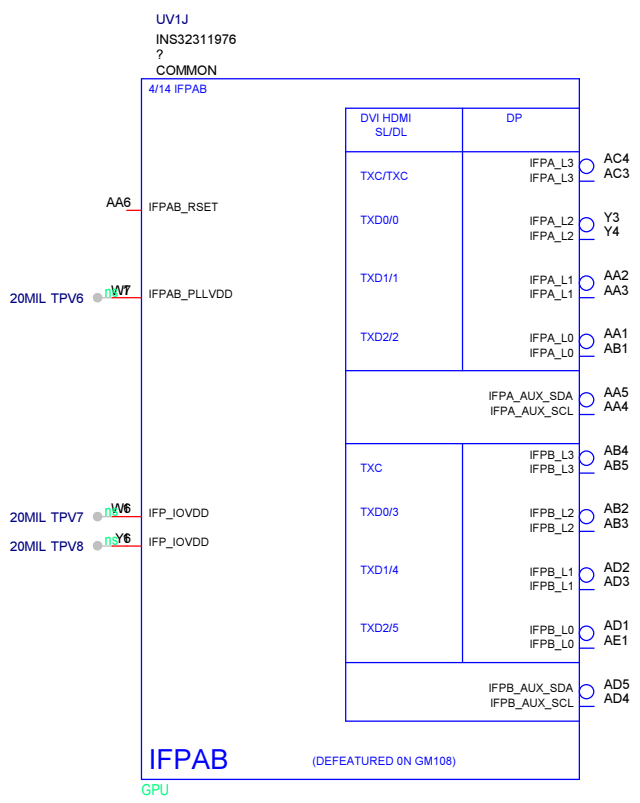
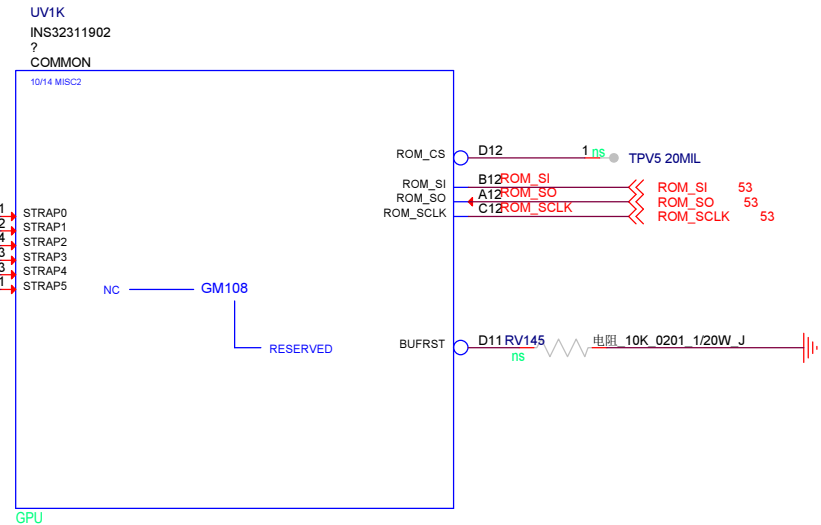
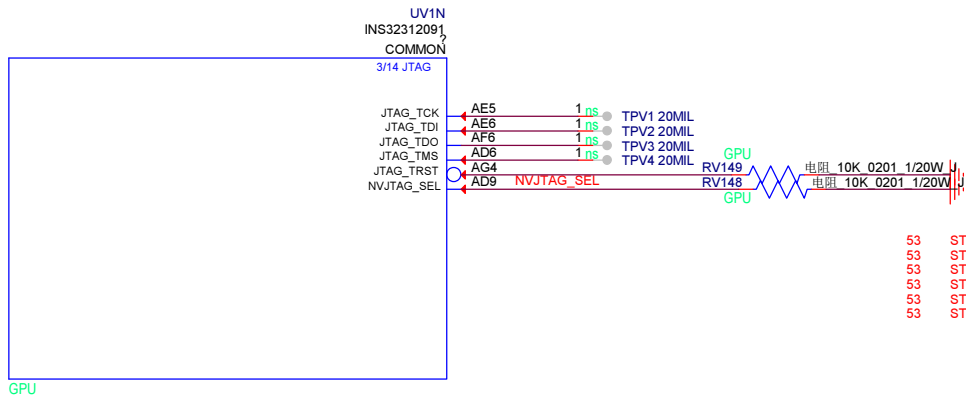


Vinafix.com

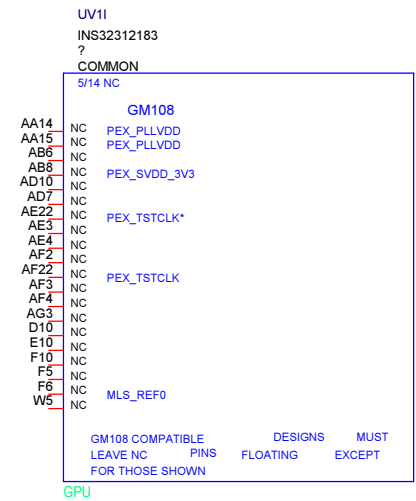


功耗板注意需开放精密电阻





Vinafix.com



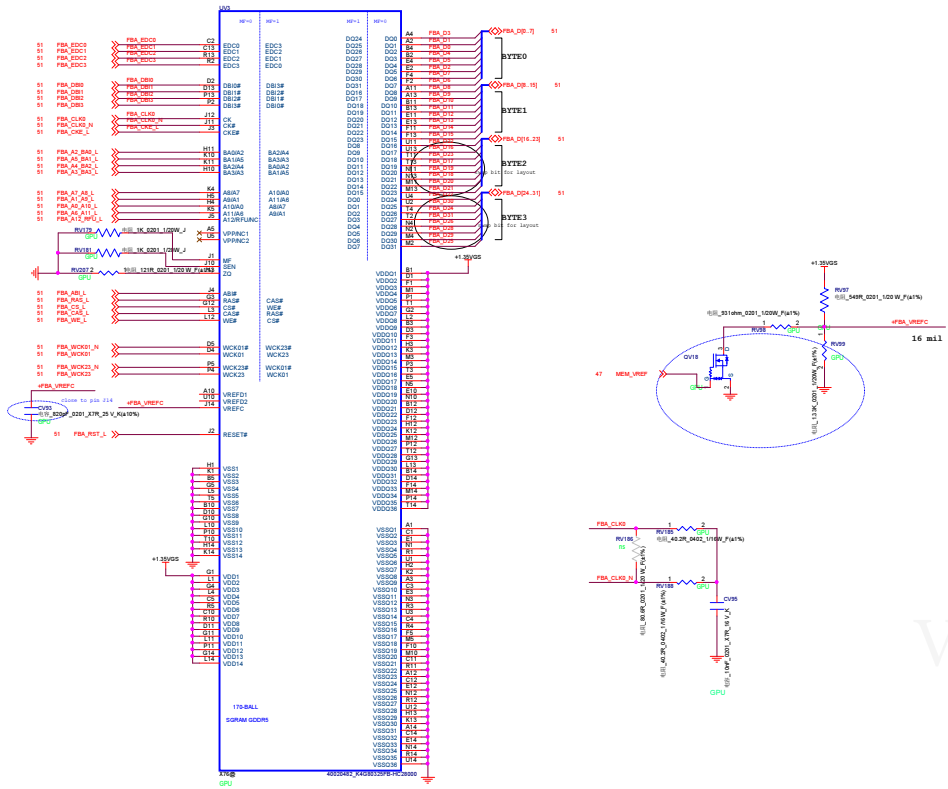


FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Size	Quantity	Placement
2C-64 (preliminary)		
6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
6S [0603]	2	
6S [0603]	1	Near GPU device
6S [0603]	3	
4C-128 (preliminary)		
6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	4	
6S [0603]	2	Near GPU device
6S [0603]	5	
B4-256		
6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	5	
6S [0603]	7	Near GPU device
6S [0603]	9	

FBVDDQ Decoupling Requirements		
	Recommended Quantity and Placement (for all supported partitions combined)	
Size	Quantity	Placement
2C-64 (preliminary)		
6S [0402]	8	Under GPU FBVDDQ ball (evenly distributed throughout partition)
6S [0603]	2	
6S [0603]	1	Near GPU device
6S [0603]	3	
4C-128 (preliminary)		
6S [0402]	12	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	4	
6S [0603]	2	Near GPU device
6S [0603]	5	
B4-256		
6S [0402]	24	Under GPU FBVDDQ ball (equally distributed across partitions)
6S [0603]	5	
6S [0603]	7	Near GPU device
6S [0603]	9	

[illegible]

Memory - Lower 32 bits



Memory - Upper 32 bits

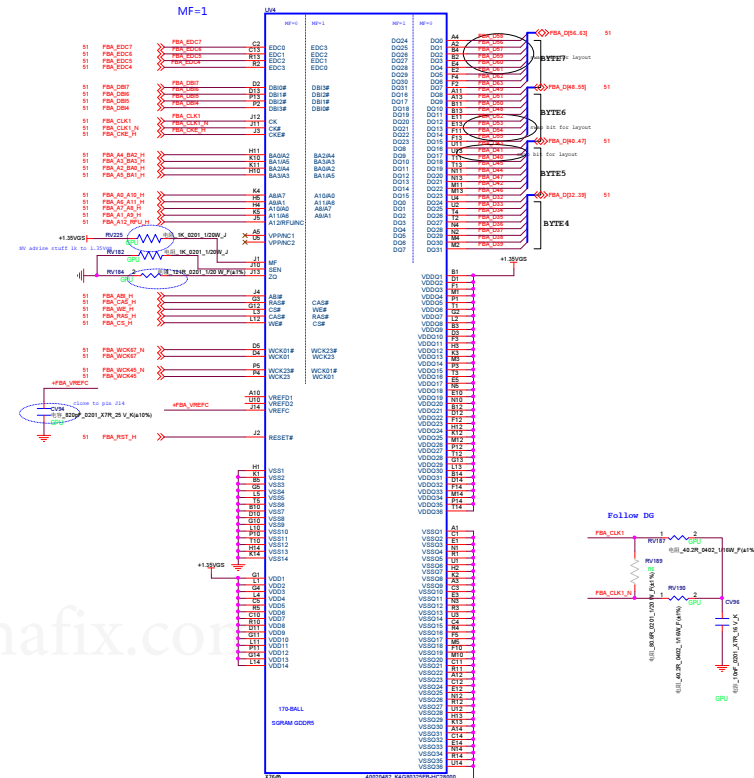
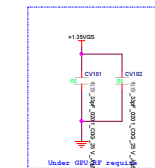
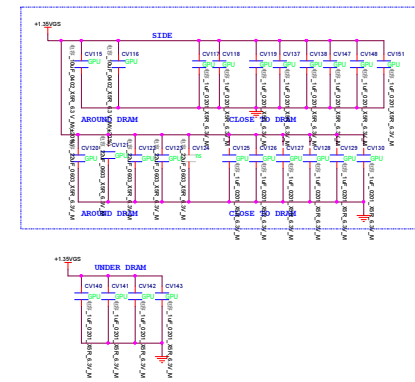
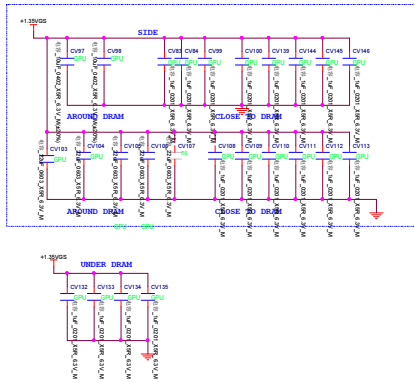
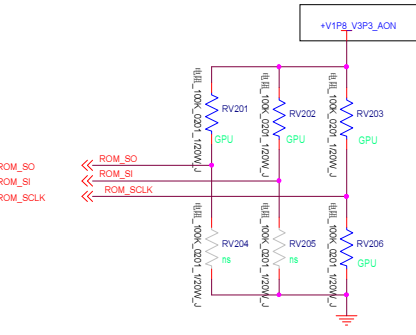
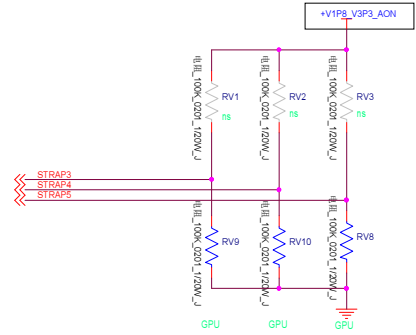
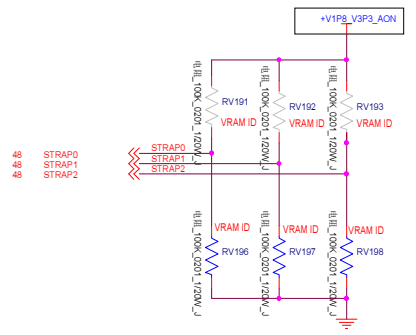


Table 9.19 DRAM-Side FBVDD/FBVDDQ Decoupling (Combined Rail)

Decoupling Capacitors		Recommended Quantity and Placement (per DRAM device)	
Capacitance	Type [Size]	Quantity	Placement (by DRAM Interface Mode)
Combined FBVDD-FBVDDQ Rail			
1.0 uF	X6S [0402]	10	For x32 DRAM: Under the DRAM FBVDD or FBVDDQ ball.
10 uF	X6S [0603]	4	For x16 DRAM in a "clamshell" PCB configuration: As close to DRAM periphery as possible. Ensure at least 2 GND vias and 2 power vias for each decoupling capacitor.
1.0 uF	X6S [0402]	8 additional	For x32 DRAM: Choose x32 interface to achieve max POR DRAM speeds. Add these additional decoupling caps under the DRAM FBVDD/Q ball; should share existing FBVDD/Q ball via if possible. See Figure 9.23 for an example.
10 uF	X6S [0603]	2	Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.
22 uF	X6S [0603]	5	For 4 GHz WCK (8 Gbps data rates): Near DRAM device. Ensure at least 2 GND vias and 2 power vias for each capacitor.





HQ PN	MPN	Strap	Vendor
HQ11121763000	H5GC8H24AJR-R2C	0xA	Hynix
HQ11121761000	MT51J256M32HF-80:B	0x9	Micron

Table 5. N175-G0/G2 GDDR5 Recommended Memories

Memory Density	Allowed Memory Configuration	FBVDD/Q	Vendor	Manufacturer Part Number	Die Revision	Strap	Memory Speed Grade	Date Code Alert
8 Gb	256Mx32 512Mx16	1.35V	Micron	MT51J256M32HF-80:B	B-die	0x9	8 Gbps	N/A
			Hynix	H5GC8H24AJR-R2C	A-die	0xA	8 Gbps	N/A

Notes:
 1. For N175-G0/G2, the maximum allowable memory case temperature is 85 °C.
 2. N175-G0/G2 running at 3.0 GHz (without intent to run 3.5 GHz at a later stage) can also use the memory configurations

SMBUS_ALT_ADDR	DEVID_SEL
0 0x9E (Default)	0 (Default)
1 0x9C (Multi-GPU usage)	1


PCIE_CFG	VGA_DEVICE
0 (Default)	0 3D Device (Class Code 302h)
1	1 VGA Device (Default)

Table 5.3 RAMCFG

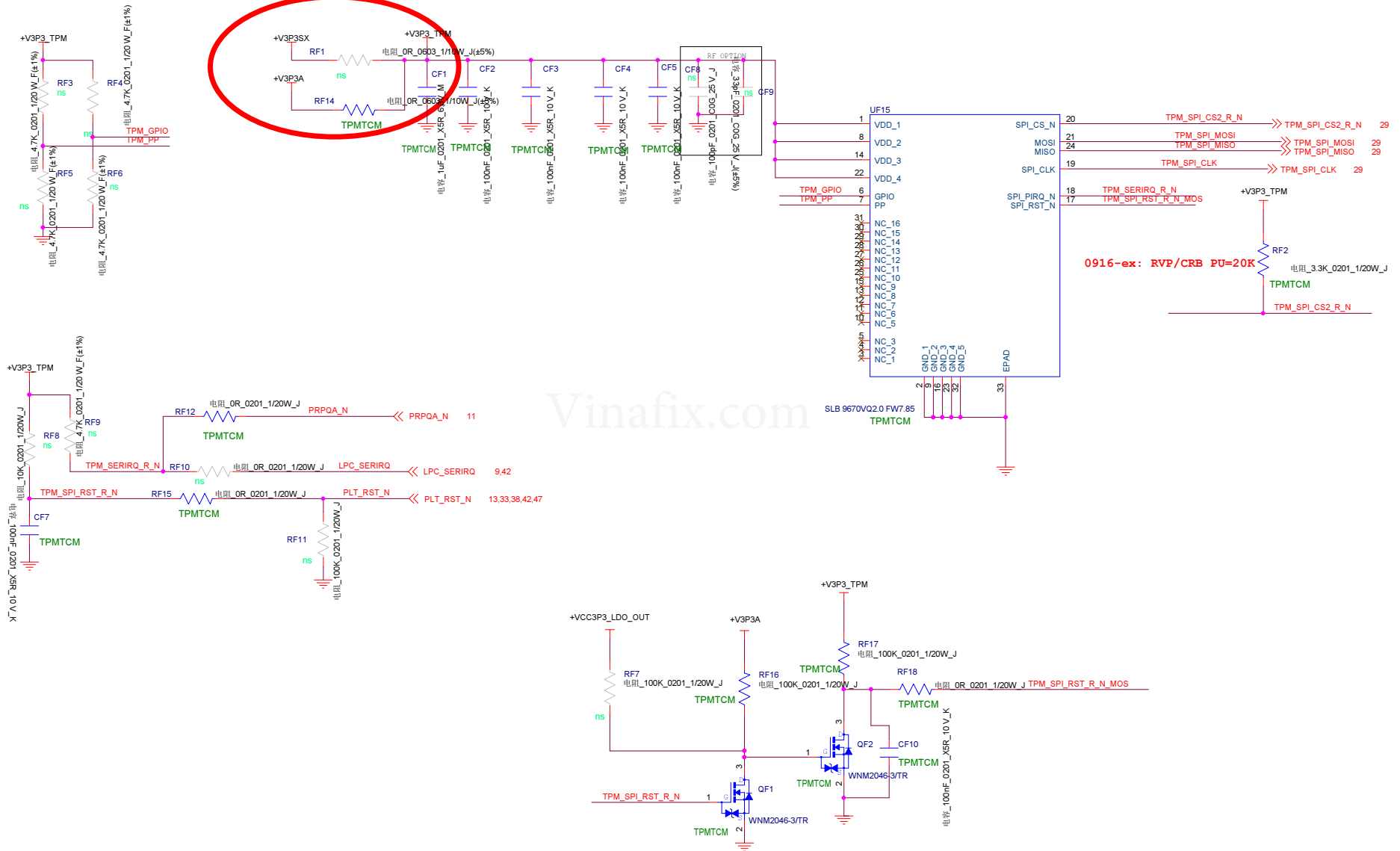
Strap Pins see Note			RAMCFG Setting Number
STRAP2	STRAP1	STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L	L	L	0 (0x0000)
L	L	H	1 (0x0001)
L	H	L	2 (0x0002)
L	H	H	3 (0x0003)
H	L	L	4 (0x0004)
H	L	H	5 (0x0005)
H	H	L	6 (0x0006)
H	H	H	7 (0x0007)
L	L	M	8 (0x0008)
L	M	L	9 (0x0009)
L	M	H	10 (0x000A)
L	H	M	11 (0x000B)
M	L	L	12 (0x000C)
M	L	H	13 (0x000D)

Physical Strapping pin	Power Rail	SOR3_EXPOSED	SOR2_EXPOSED	SOR1_EXPOSED	SOR0_EXPOSED
ROM_SCLK	M	Disable	Disable	Disable	Disable
ROM_S1	H				
ROM_S0	H				

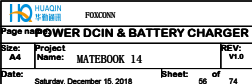
Vinafix.com

 HUAQIN 华勤通信		FOXCONN	
Page name: ALS			
Size: A4	Project Name: MATEBOOK 14		REV: V1.0
Date: <u>Saturday, December 15, 2018</u>		Sheet: 54 of 74	

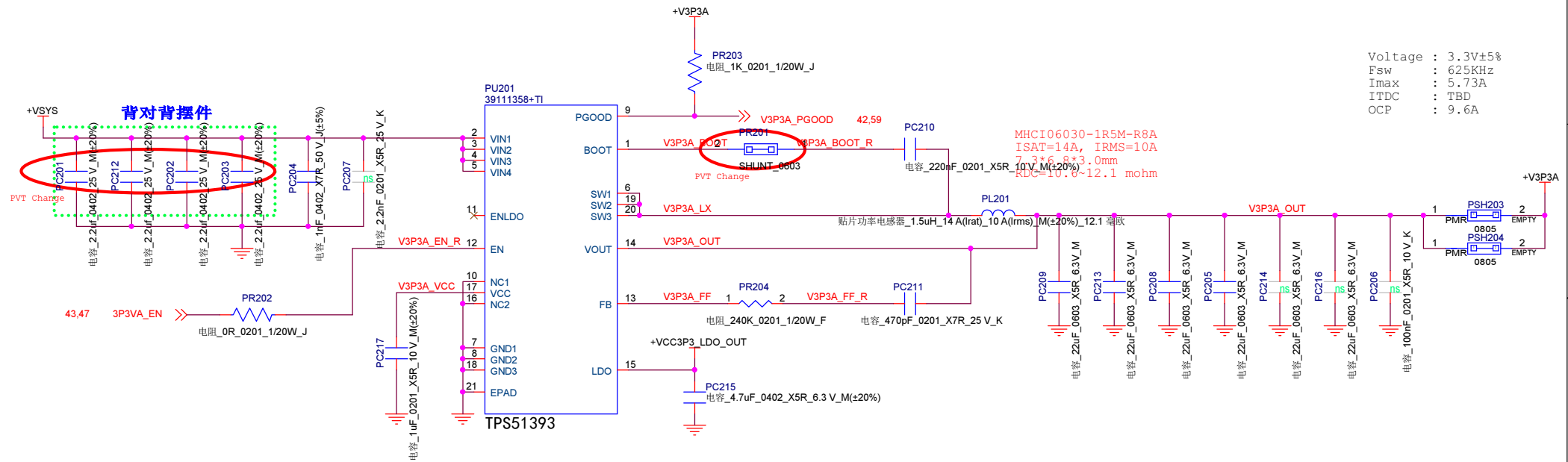
to check the PWR well
for TPM/TCM to avoid
leakage, to +V3P3A?




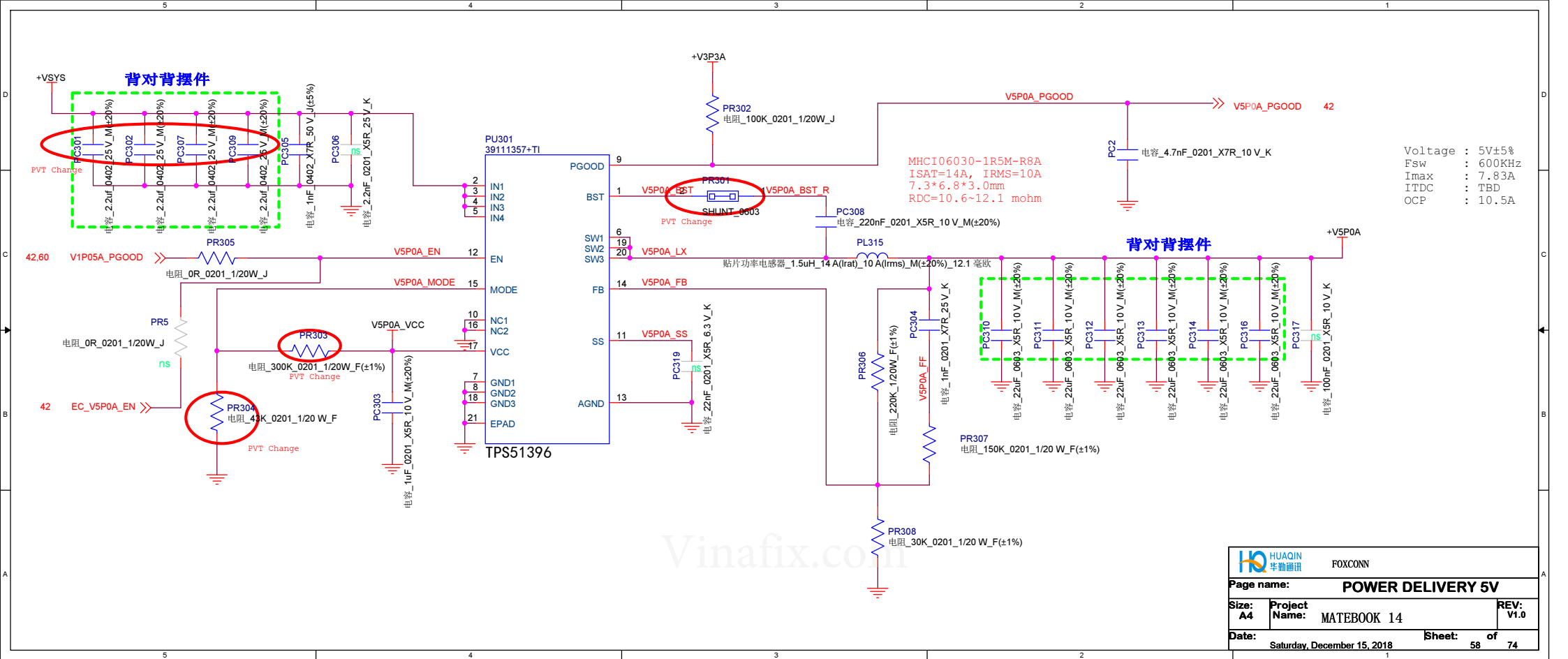
Charger



+V3P3A

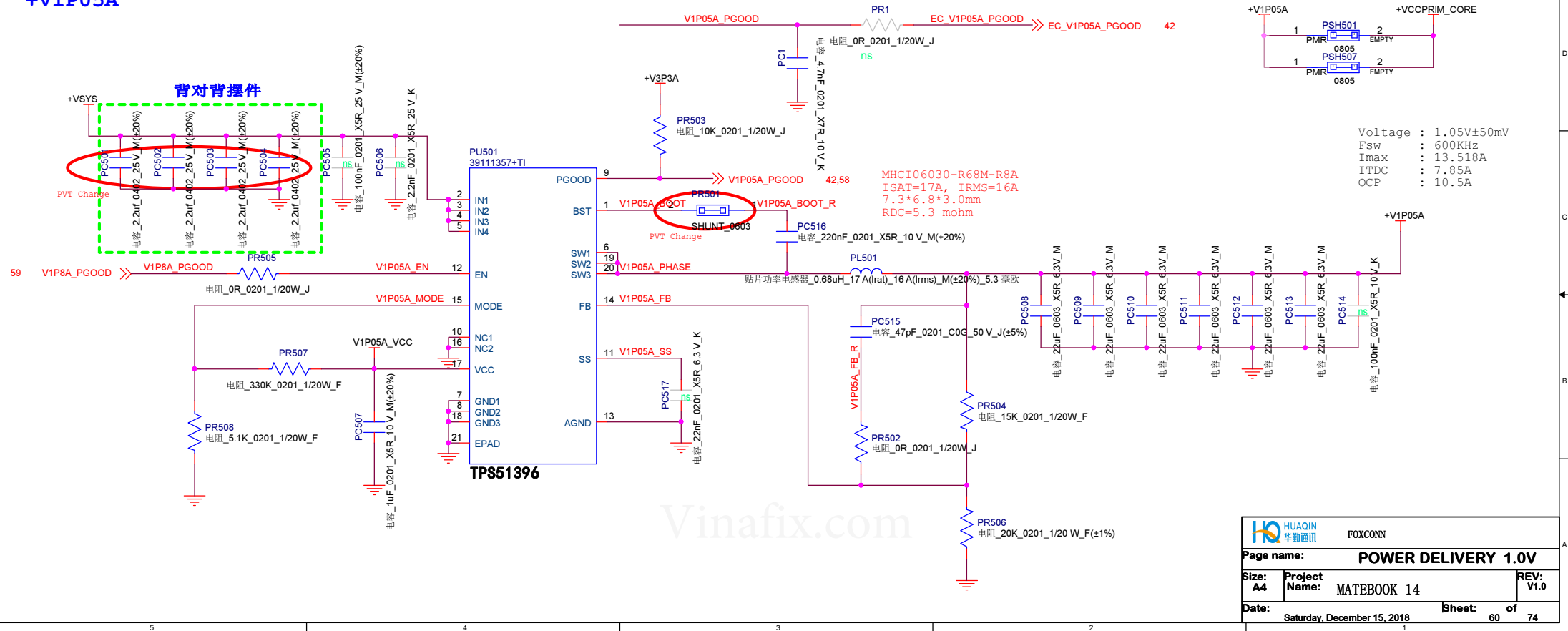



 HUAQIN 华勤通讯		FOXCONN	
Page name:		POWER DELIVERY 3.3V	
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 57	of 74	

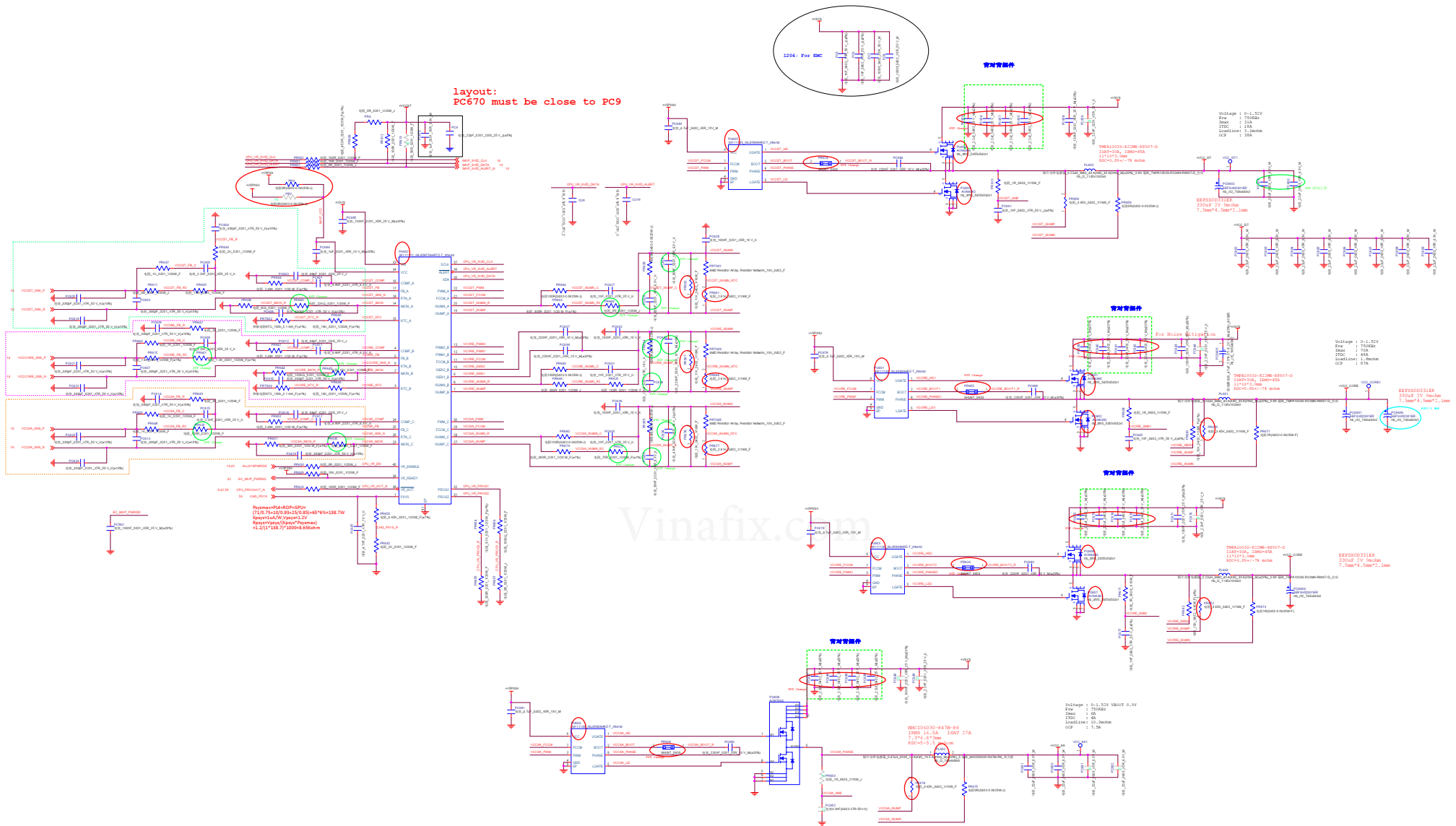


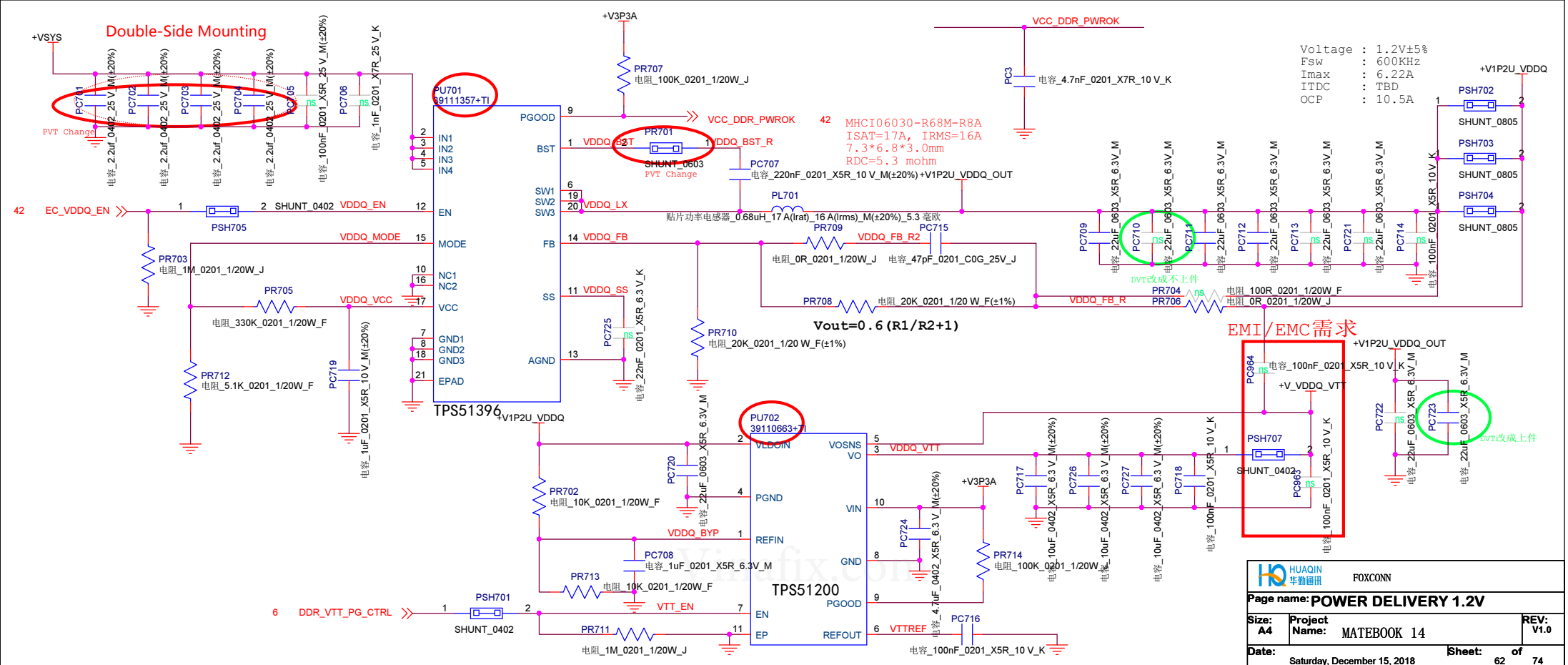
+V1P05A

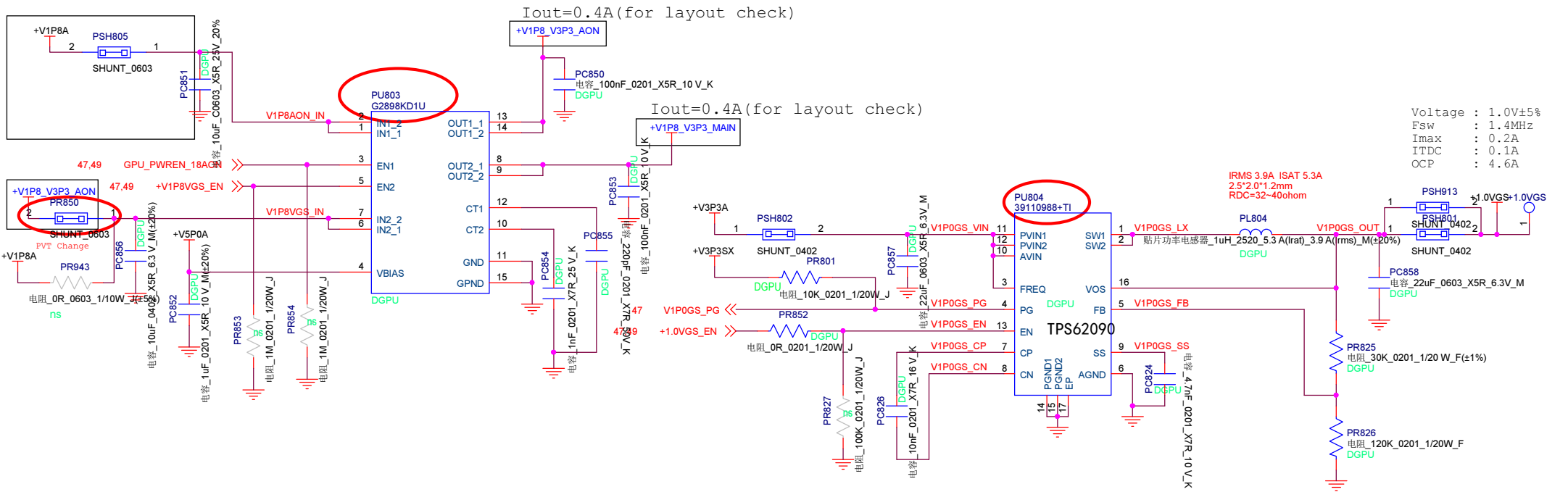
背对背摆件




 HUAQIN 华勤通讯		FOXCONN	
Page name: POWER DELIVERY 1.0V			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 60		of 74



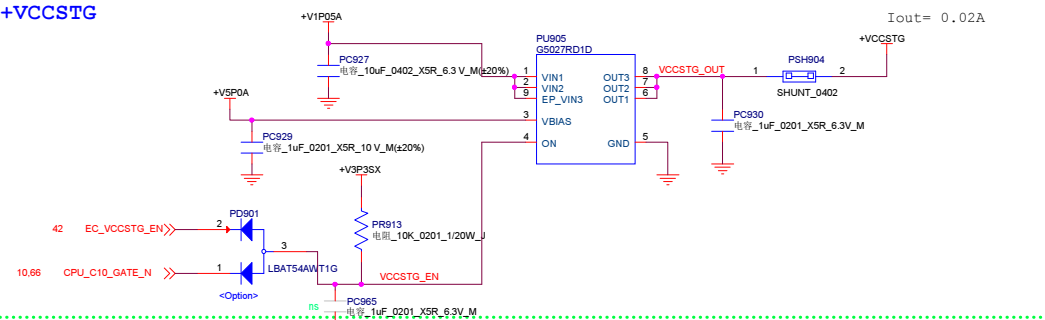




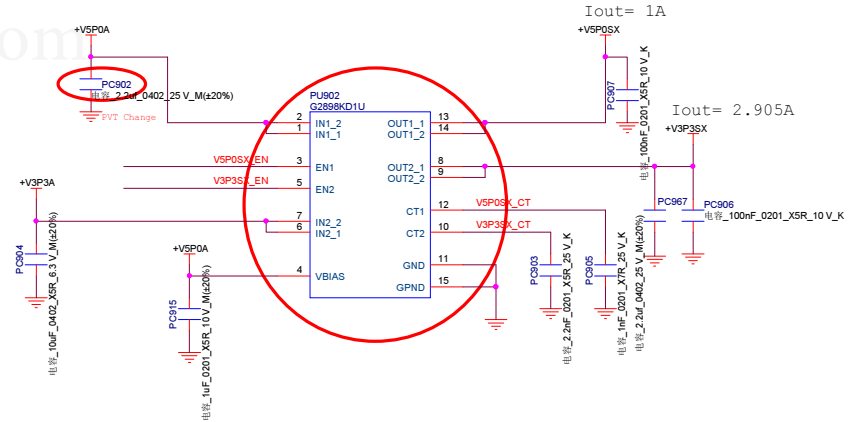
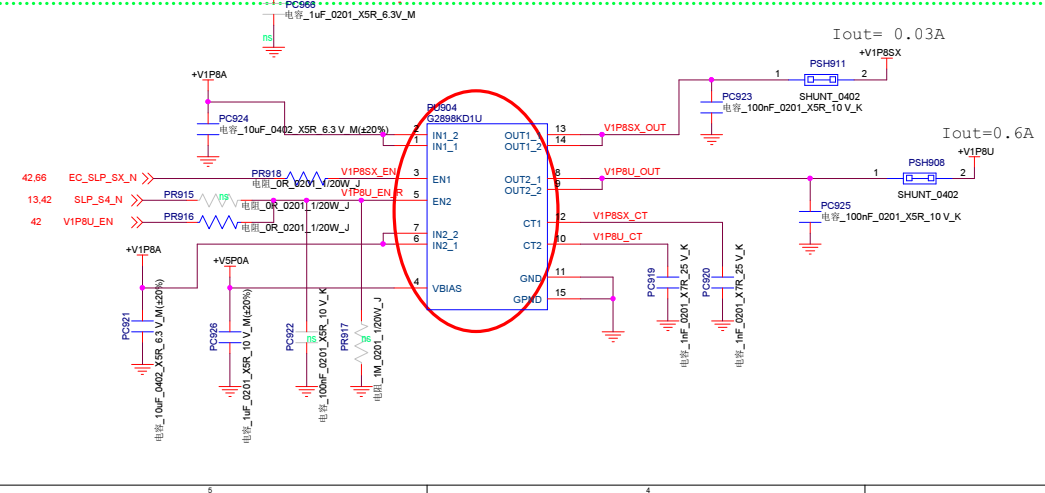
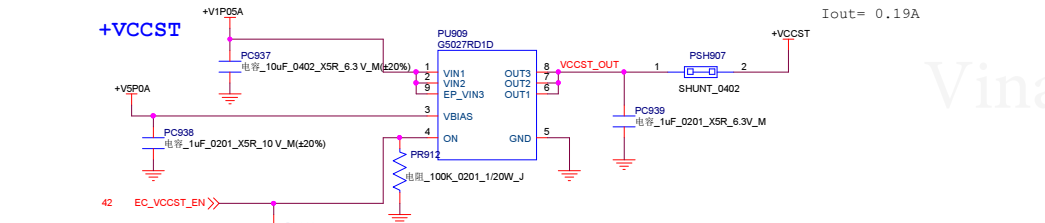
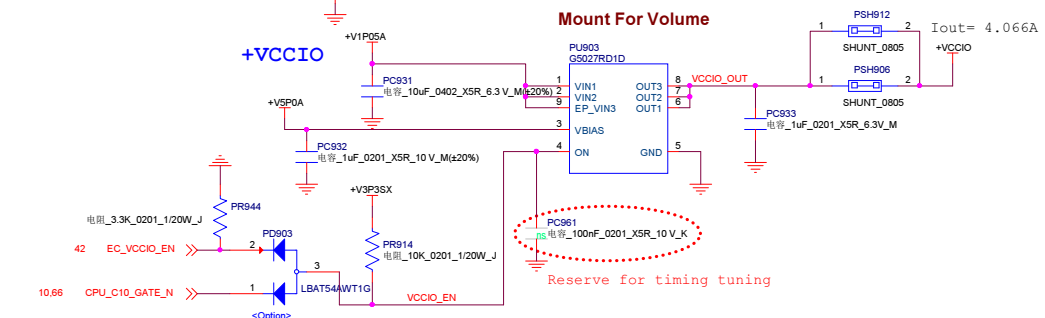
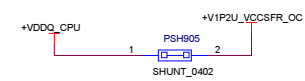
Vinafix.com

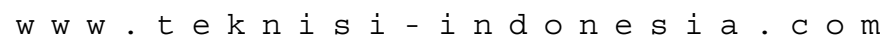
 HUAQIN 华勤通讯		FOXCONN	
Page name: POWER DELIVERY 1.0VGS&1.8VGS			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 64	of 74	

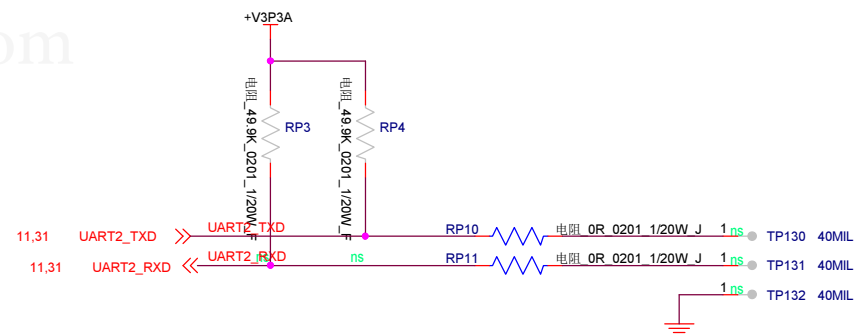
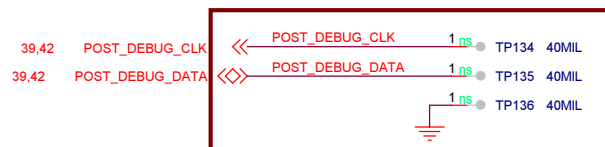
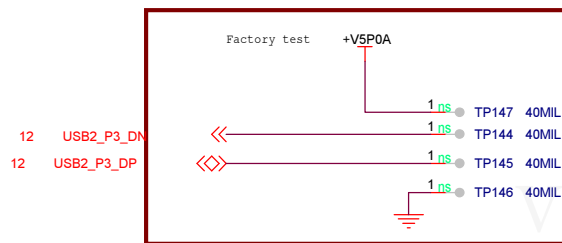
+VCCSTG

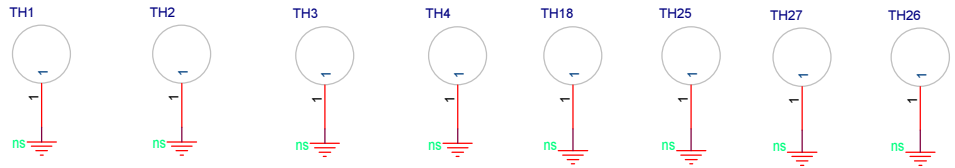


+V1P2U_VCCSFR_OC

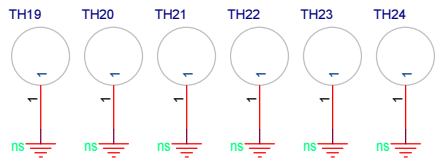




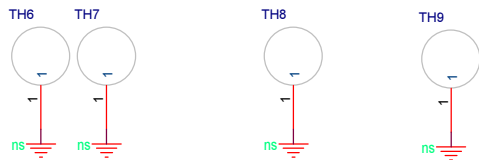
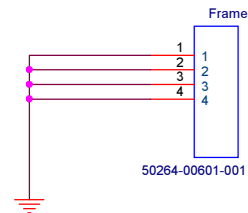





nb_pthc2d5hc4d6 数量: 3
nb_pthc3hc6 数量: 1
nb_pthc1d9hc4d5 数量: 1
nb_pthc1d9hc4 数量: 1
nb_pthc1d9hc3d5 数量: 1
nb_pthc1d9hc4 数量: 1



nb_pth3d4hc4d4 数量: 6




nb_pthc3d2htc5d2bc6 数量: 2
nb_pthc2d8hc4d4 数量: 1
nb_pthc1d8htc5d5bc4d5 数量: 1

 HUAQIN 华勤通讯		FOXCONN	
Page name: Hole & Mark			
Size: A4	Project Name: MATEBOOK 14	REV: V1.0	
Date: Saturday, December 15, 2018	Sheet: 69	of 74	

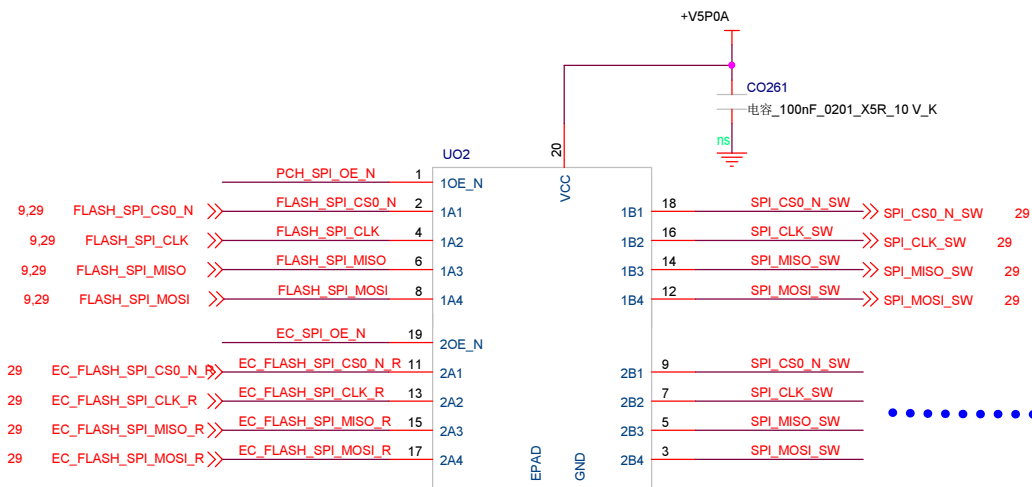
5	4	3	2	1
D				D
C				C
B				B
A				A

Vinafix.com

 HUAQIN 华勤通讯		FOXCONN	
Page name: Changelist			
Size: A4	Project Name: MATEBOOK 14		REV: V1.0
Date: Saturday, December 15, 2018	Sheet: 70		of 74

Rvsd For PCH and EC SPI Isolation

0918-ex:
From PCH



0918-ex:
From EC

